

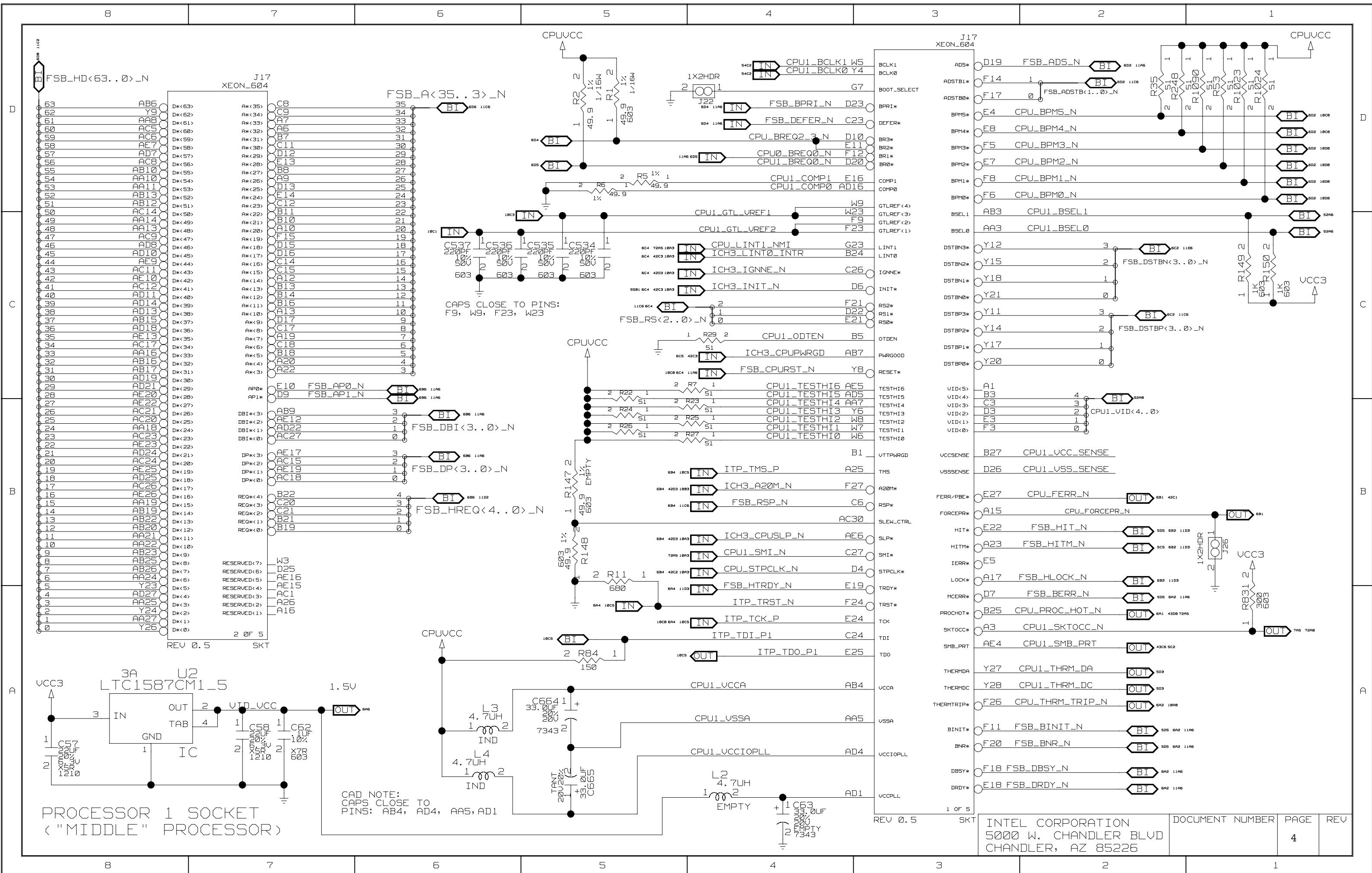
DUAL INTEL® XEON™ PROCESSOR / E7501 CHIPSET
EVALUATION KIT BOARD SCHEMATICS
REV B1

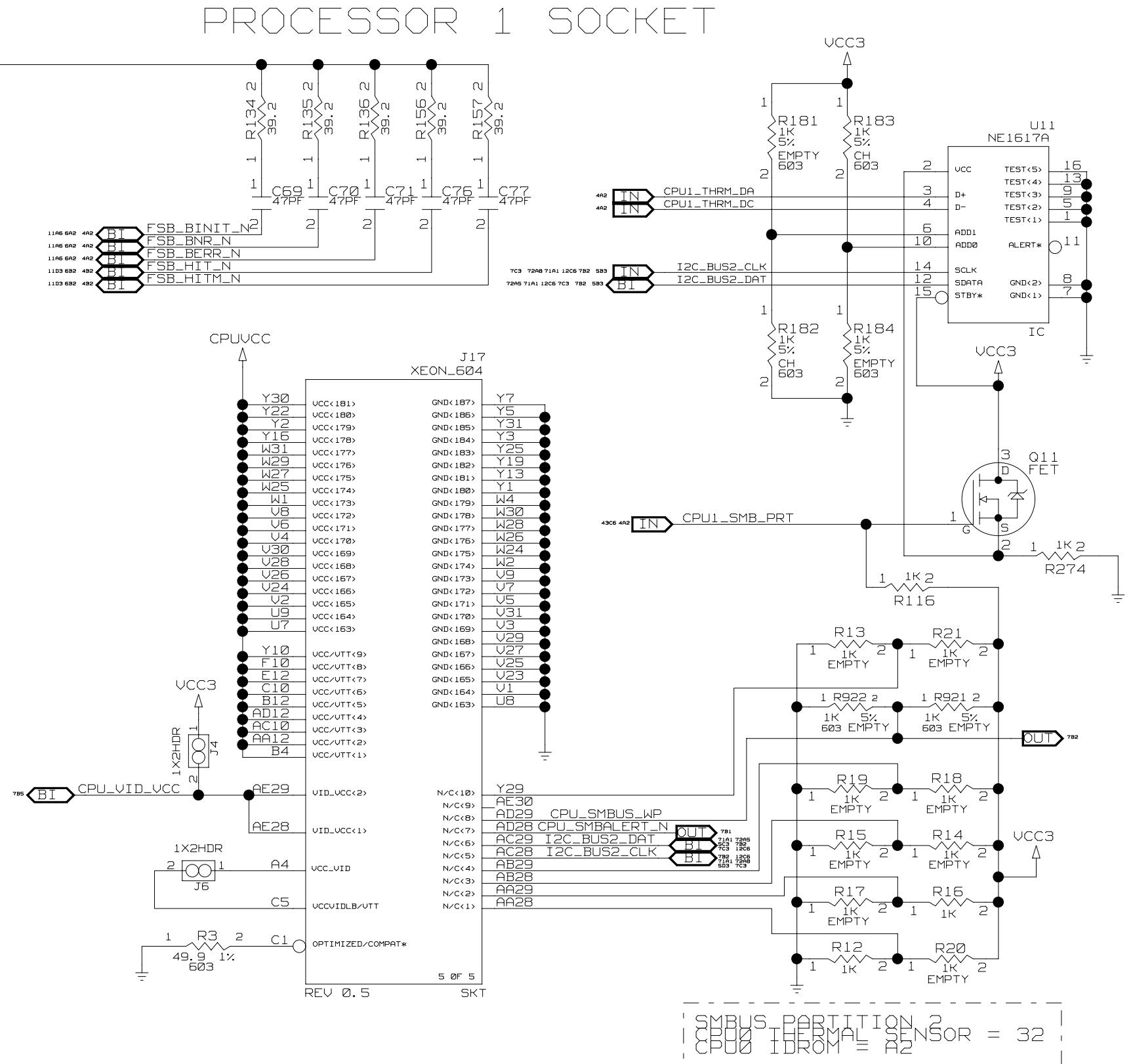
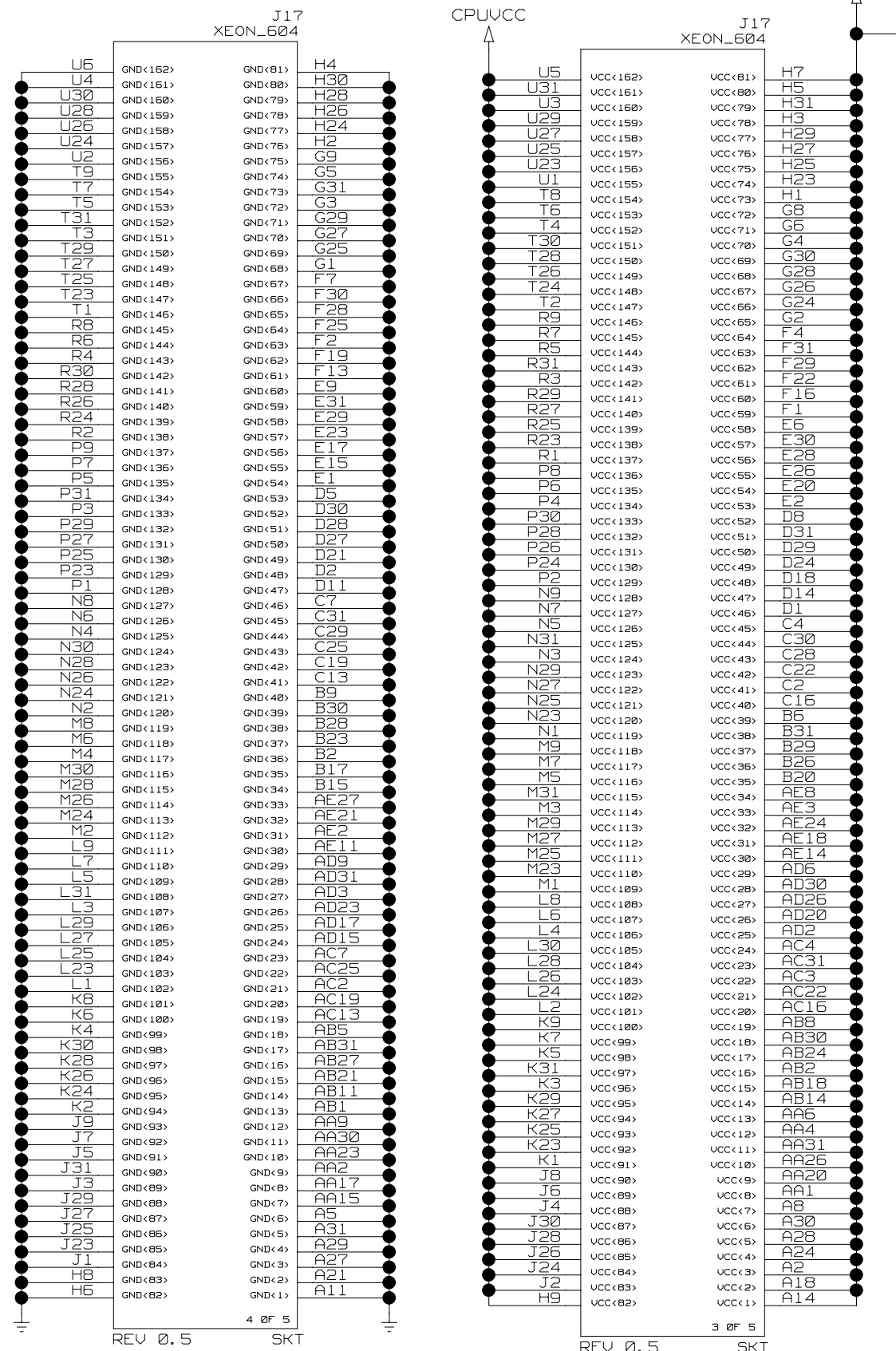
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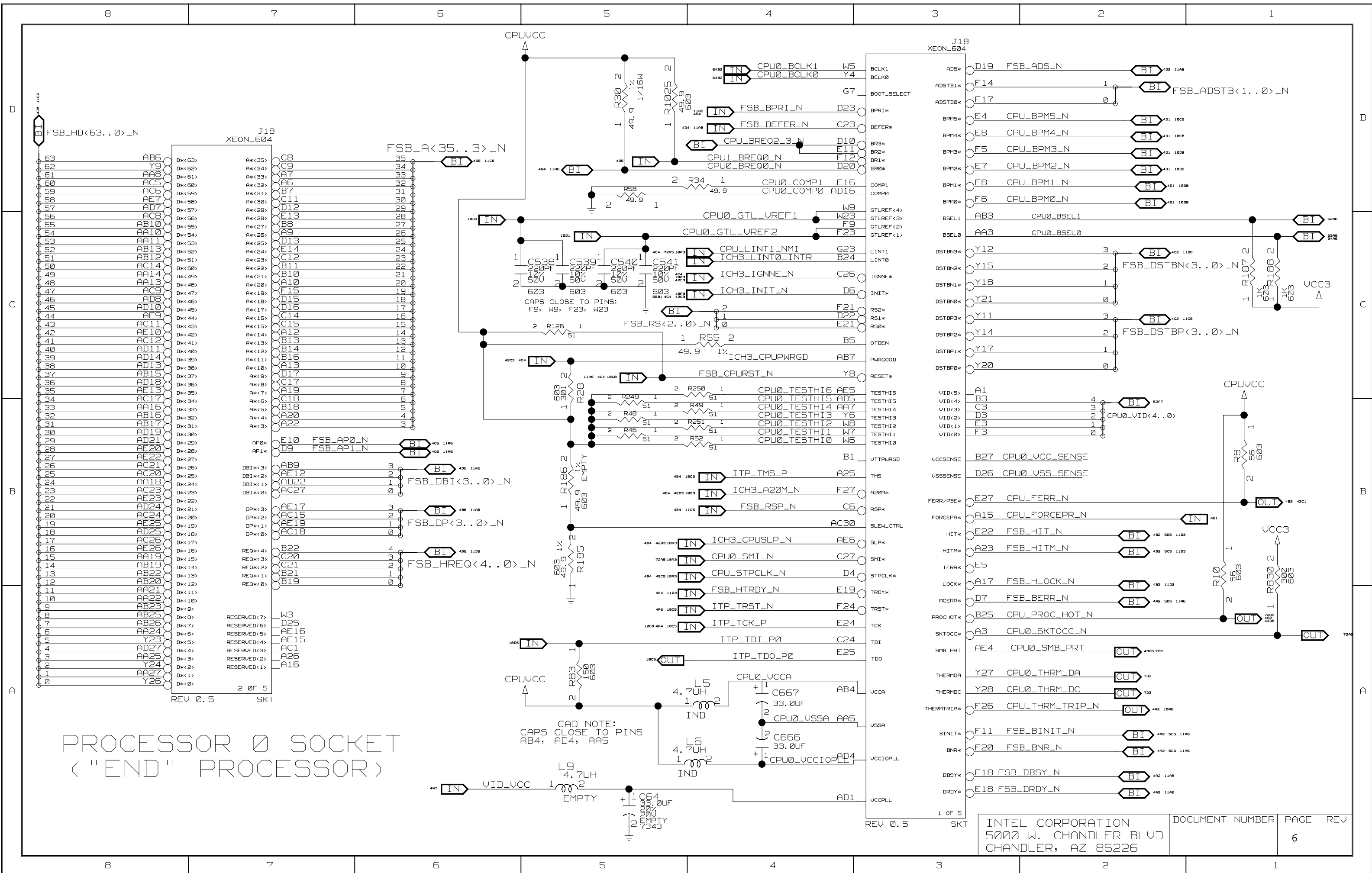
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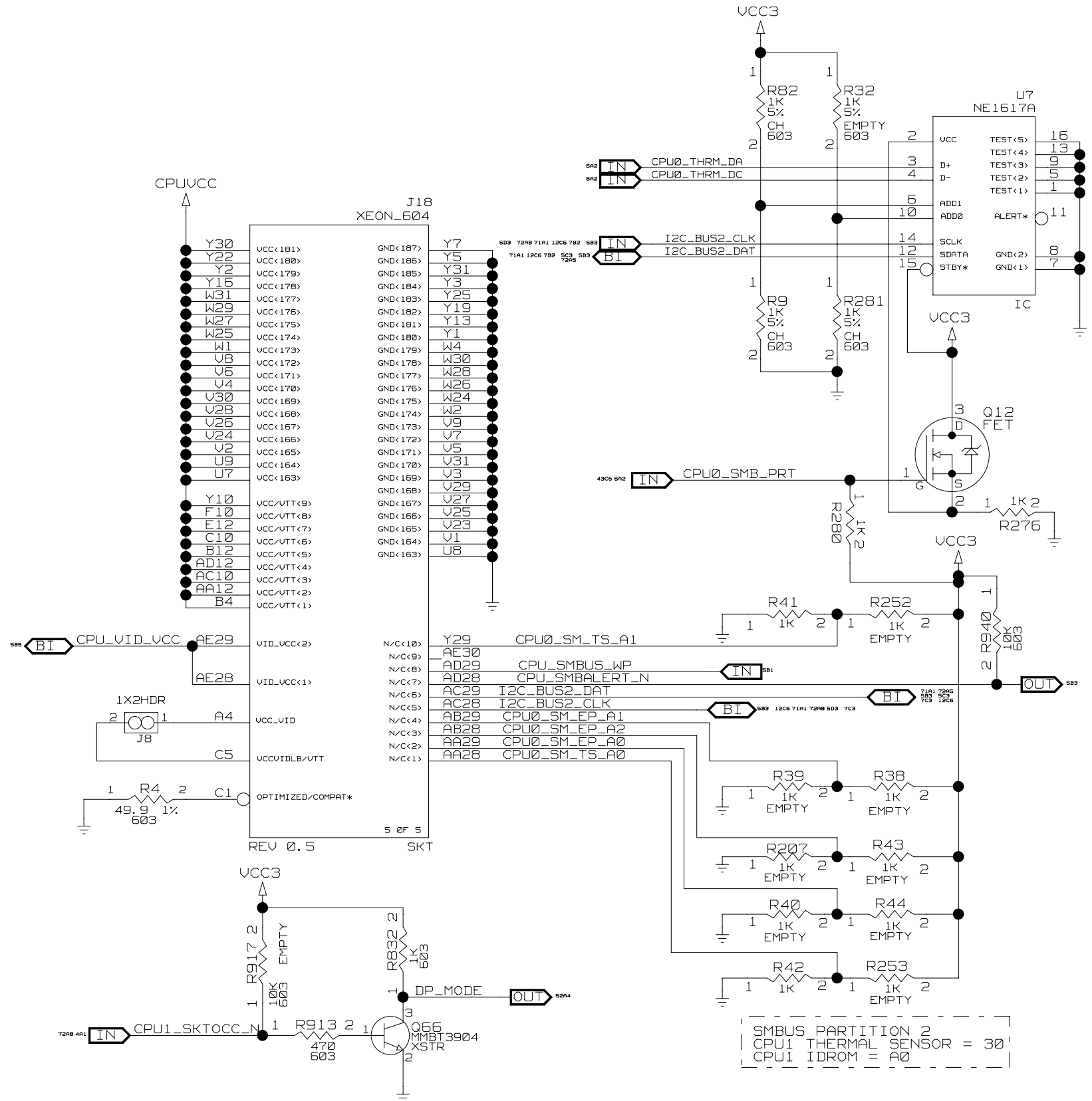
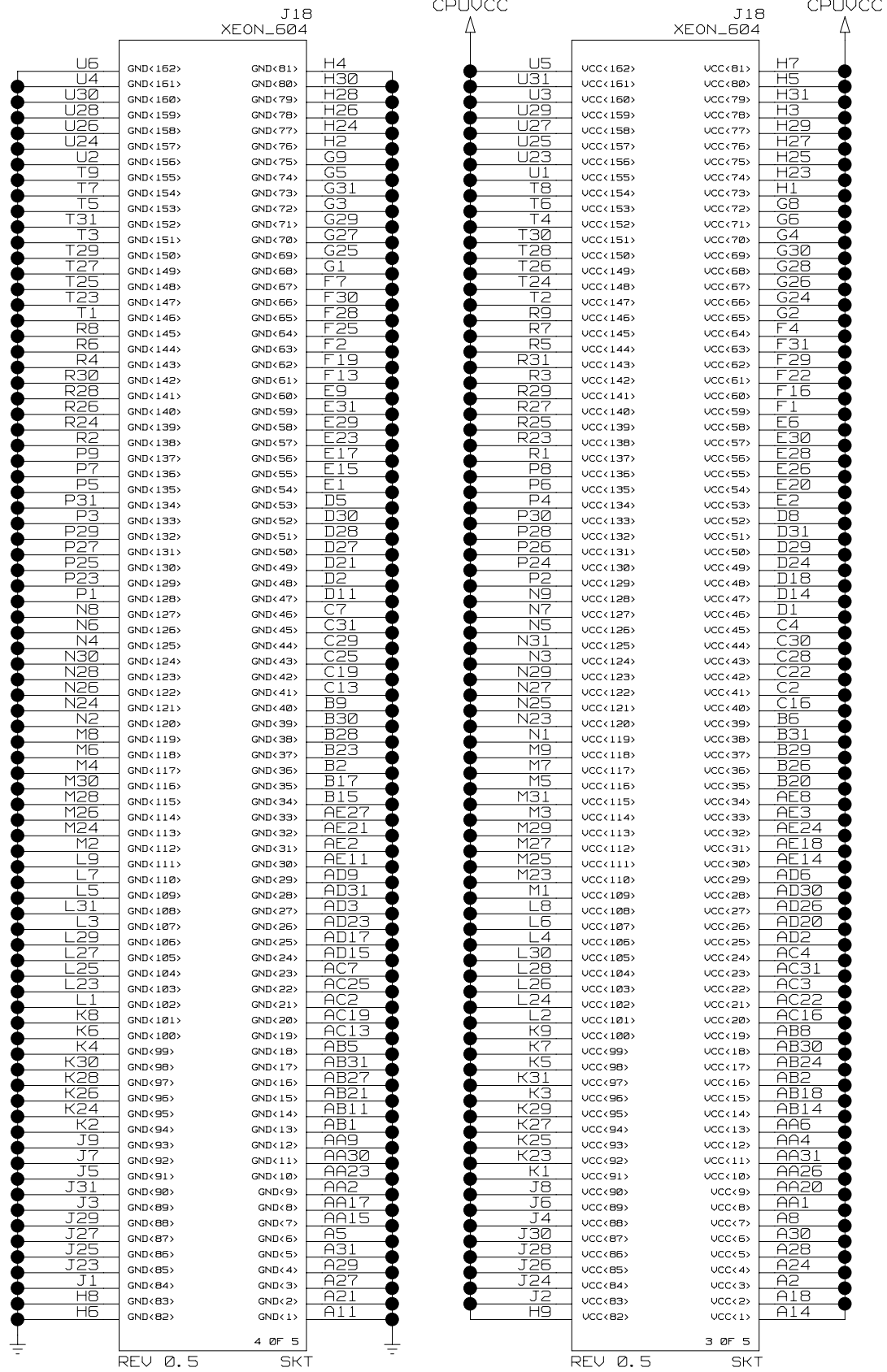
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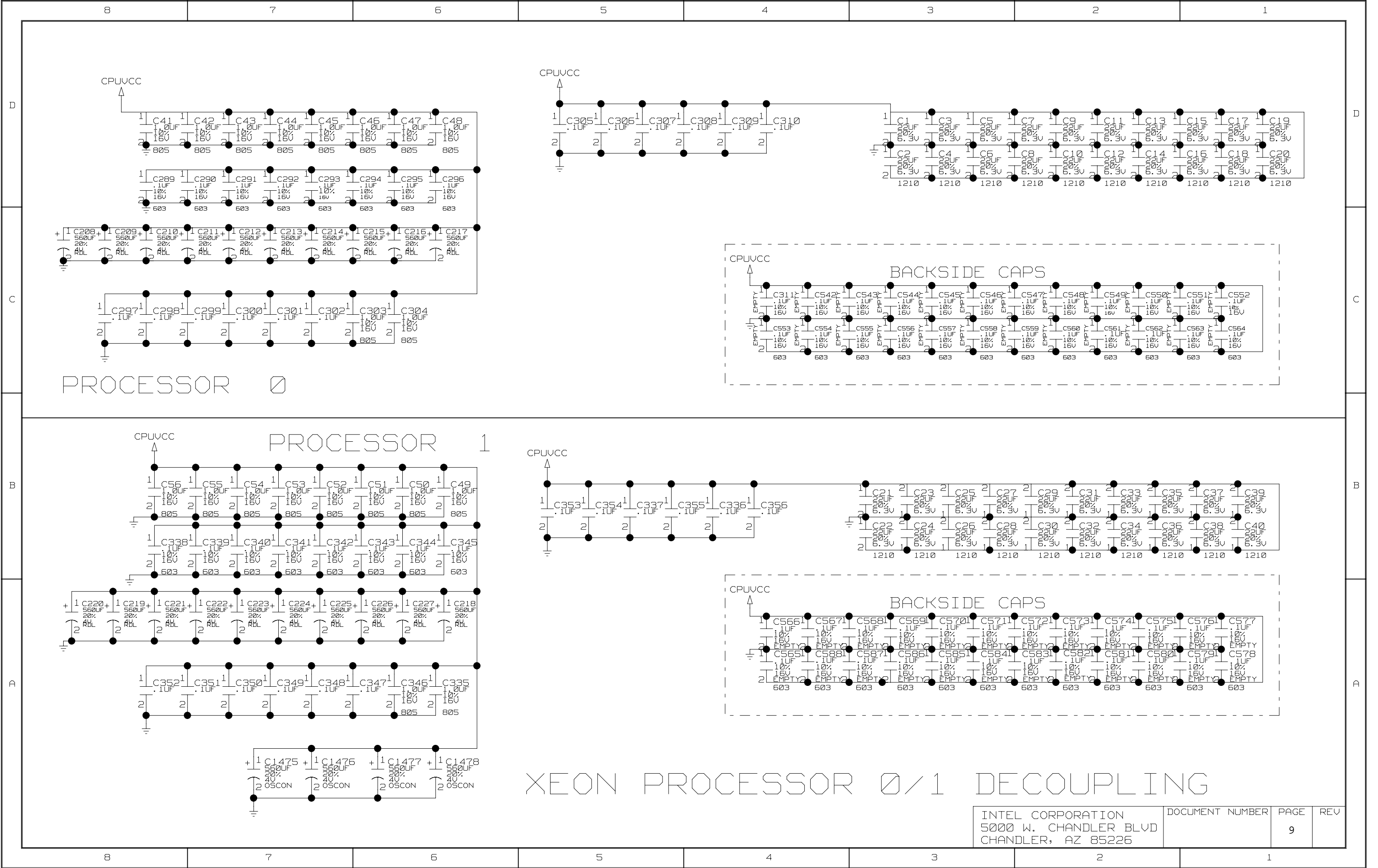


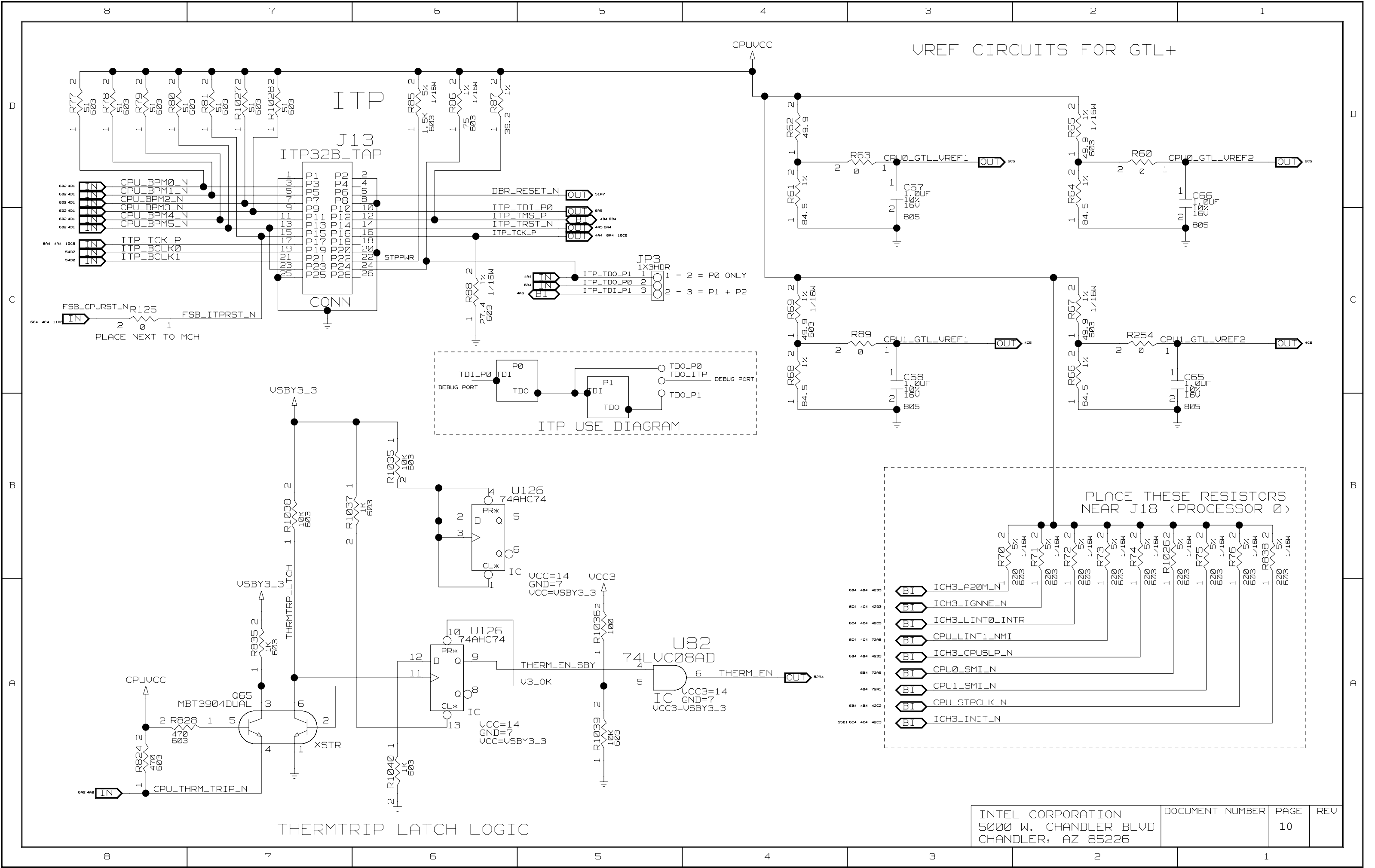


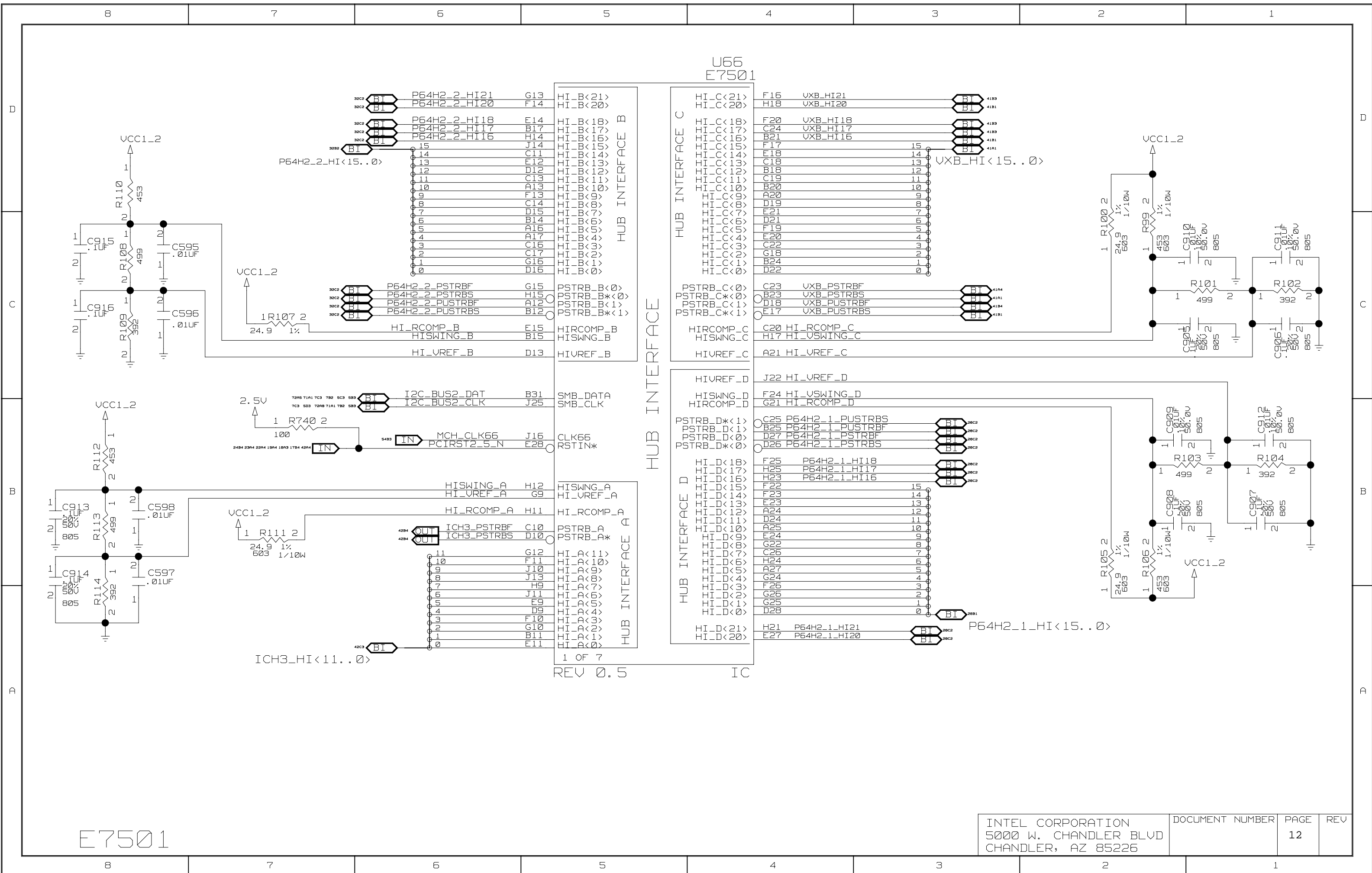
PROCESSOR ☐ SOCKET

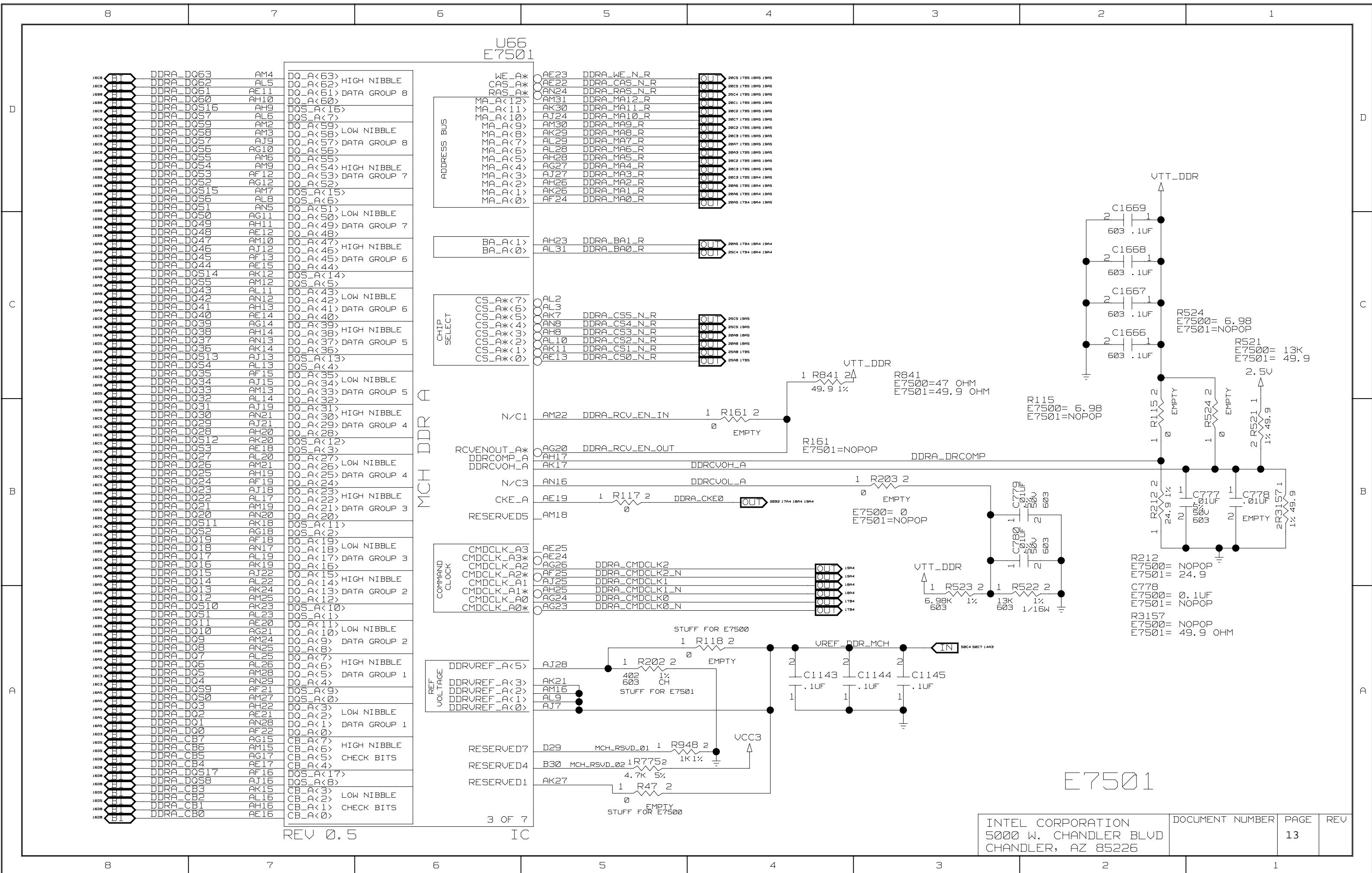


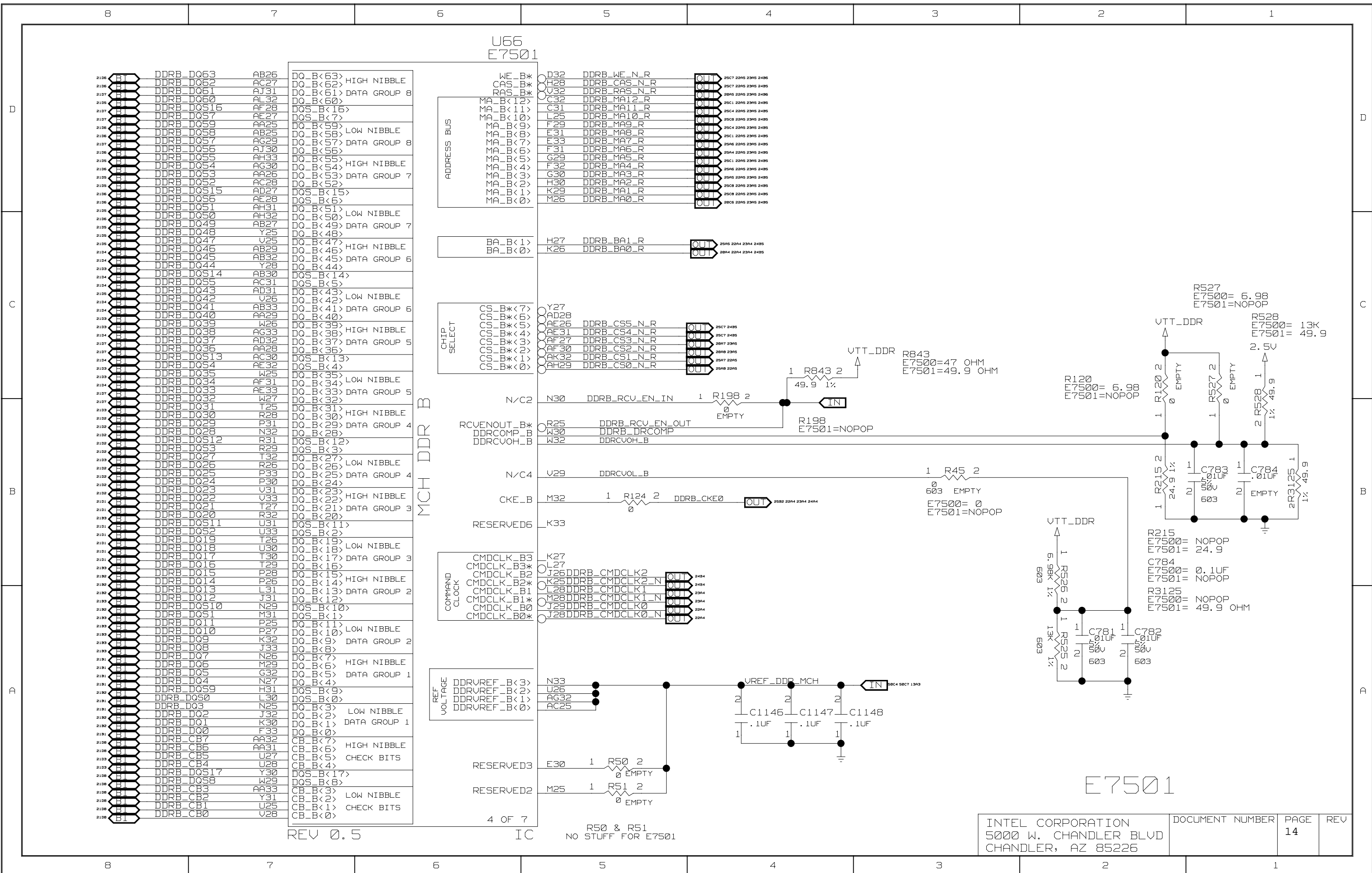
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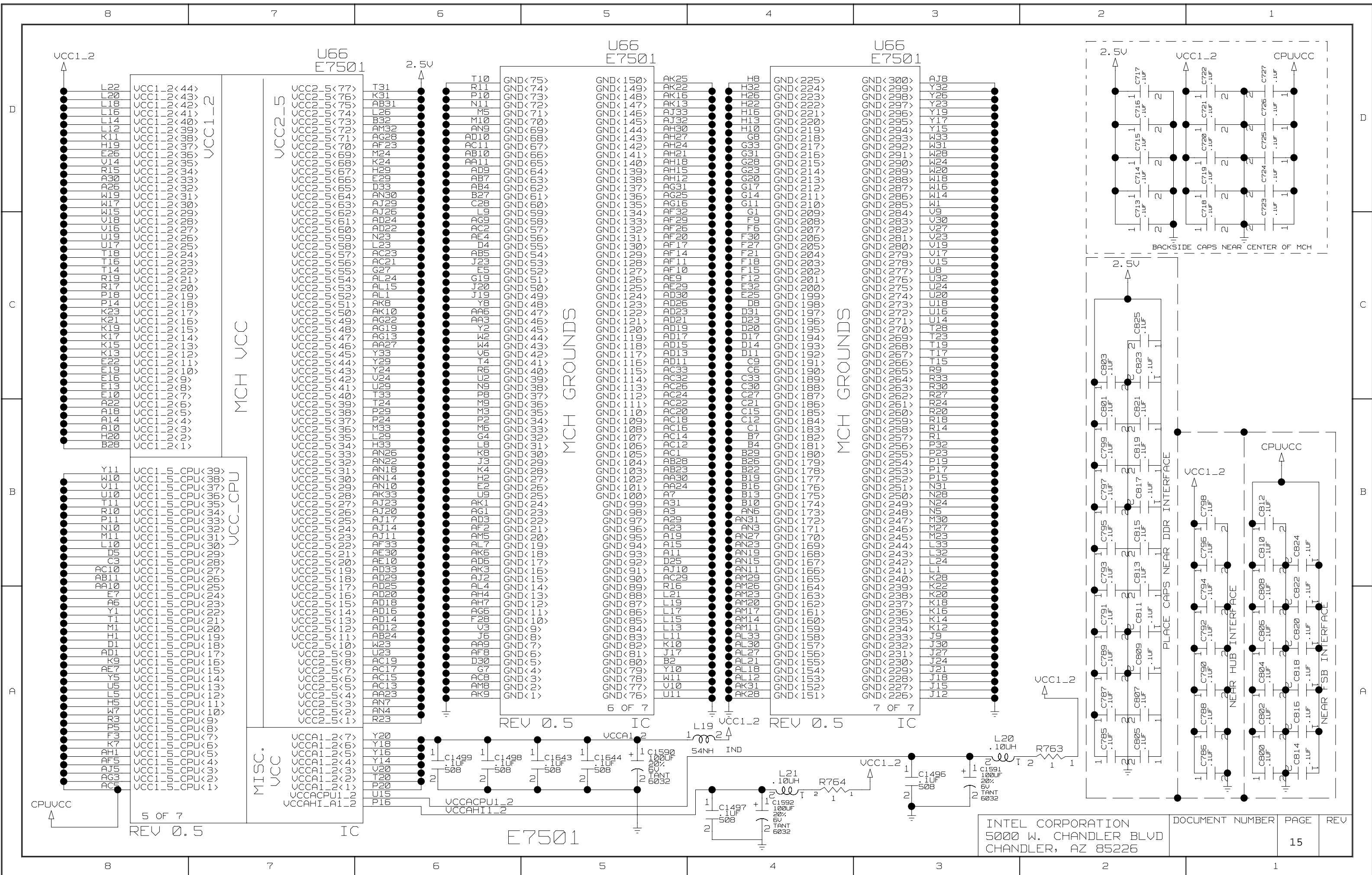






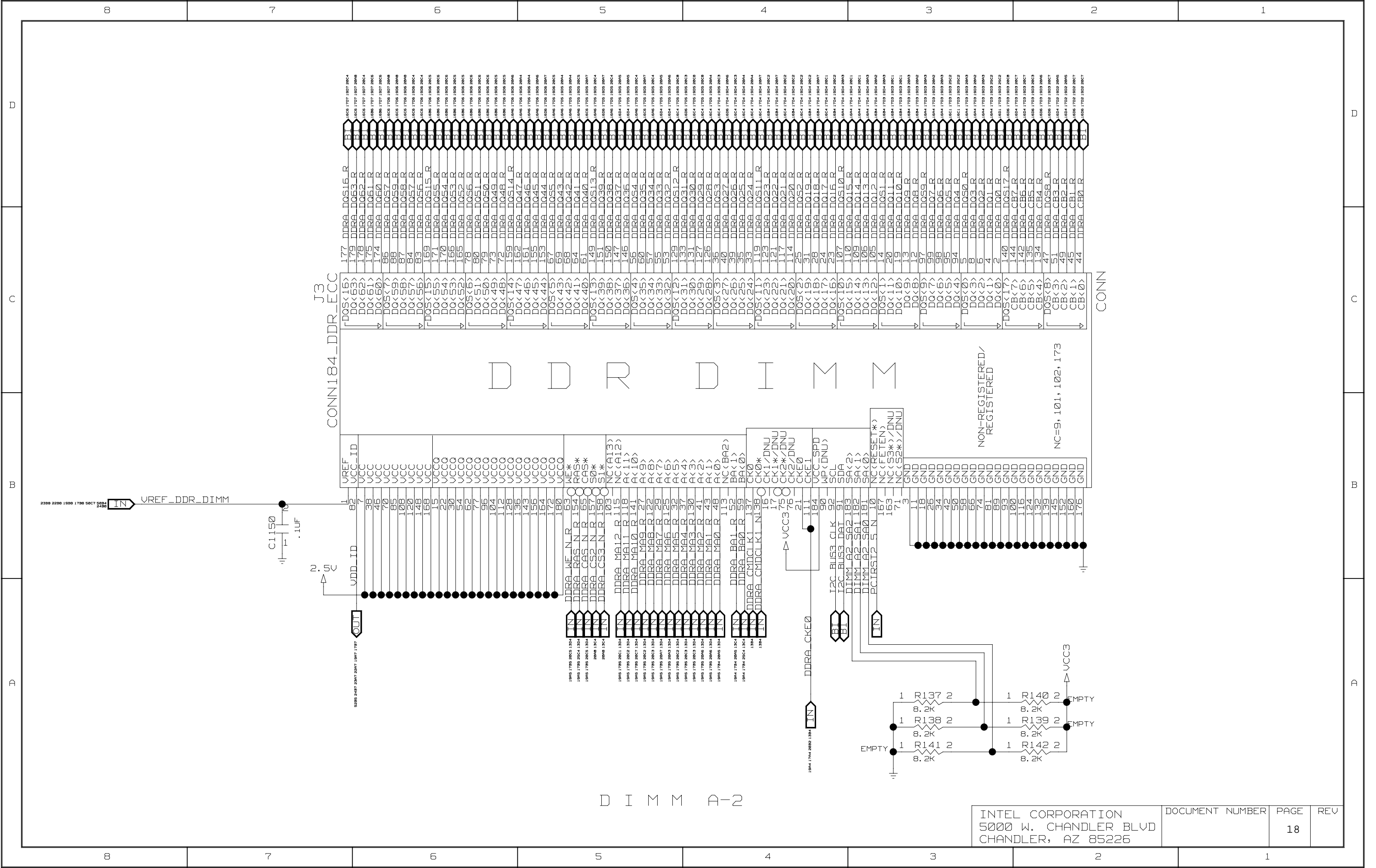




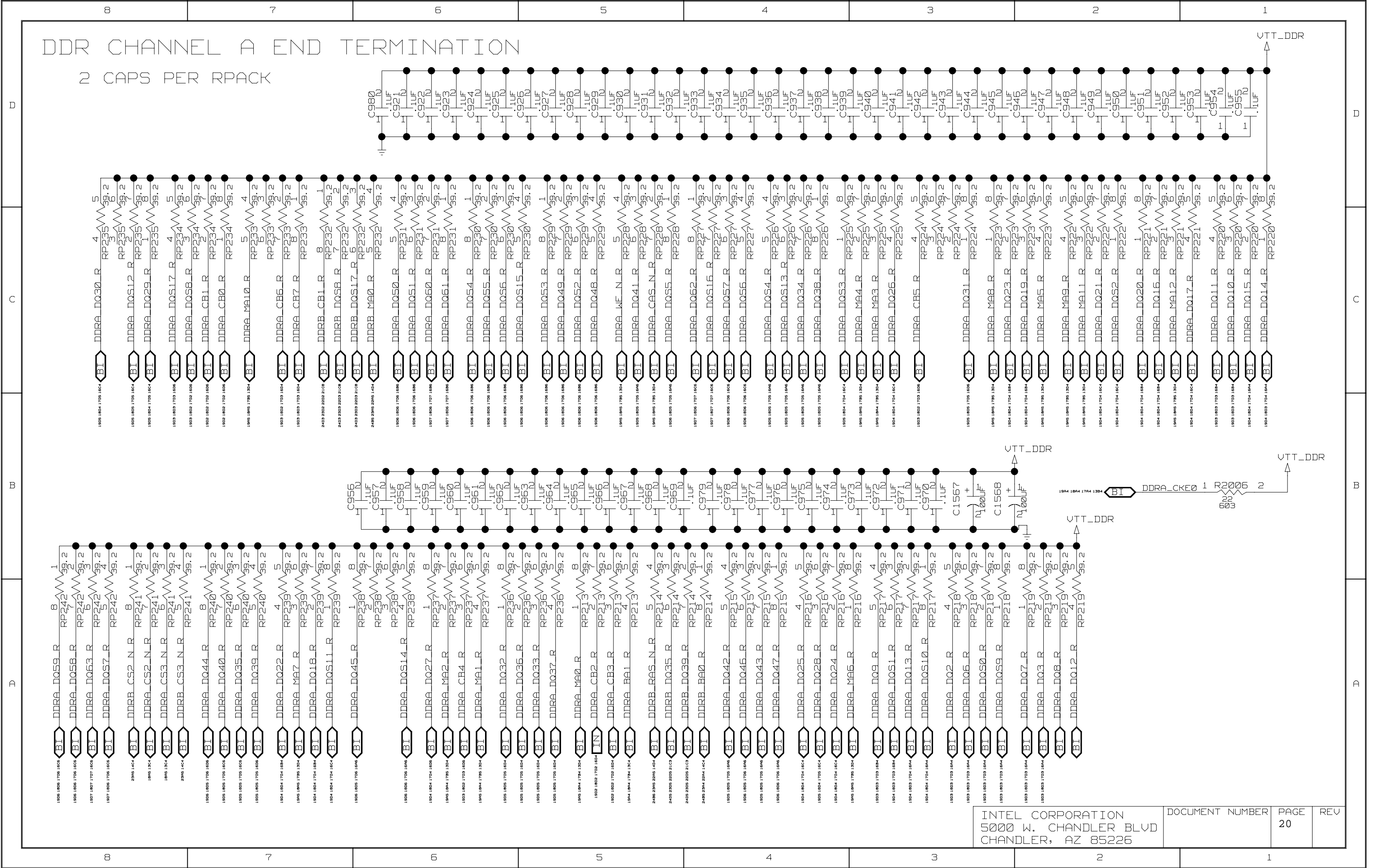




D I M M A-1







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BI

DDRA_DQ59_R

RP242

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BI

DDRA_DQ58_R

RP242

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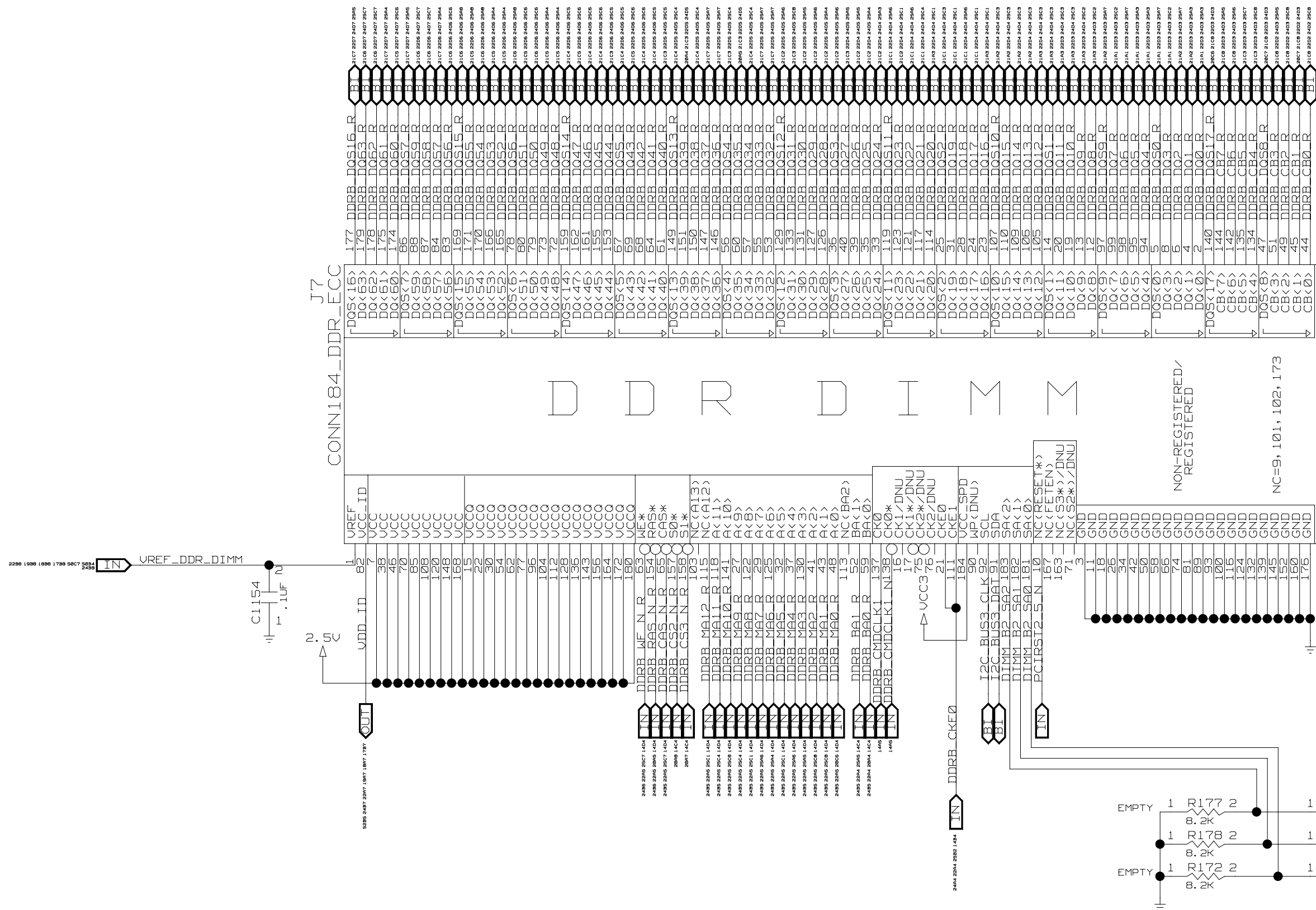
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NON-REGISTERED/
REGISTERED

NC=9, 101, 102, 173

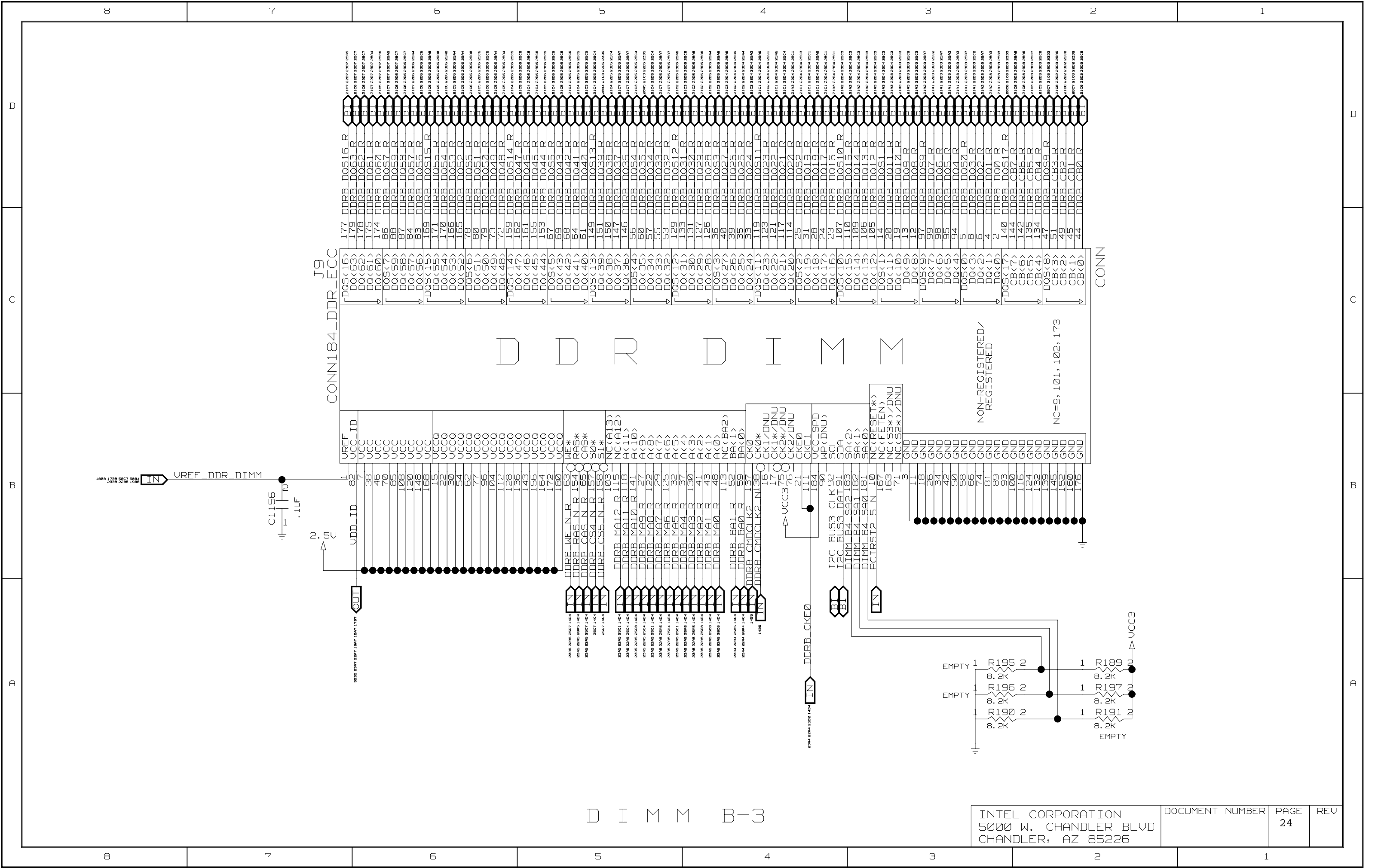
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CHANDLER, AZ 85226

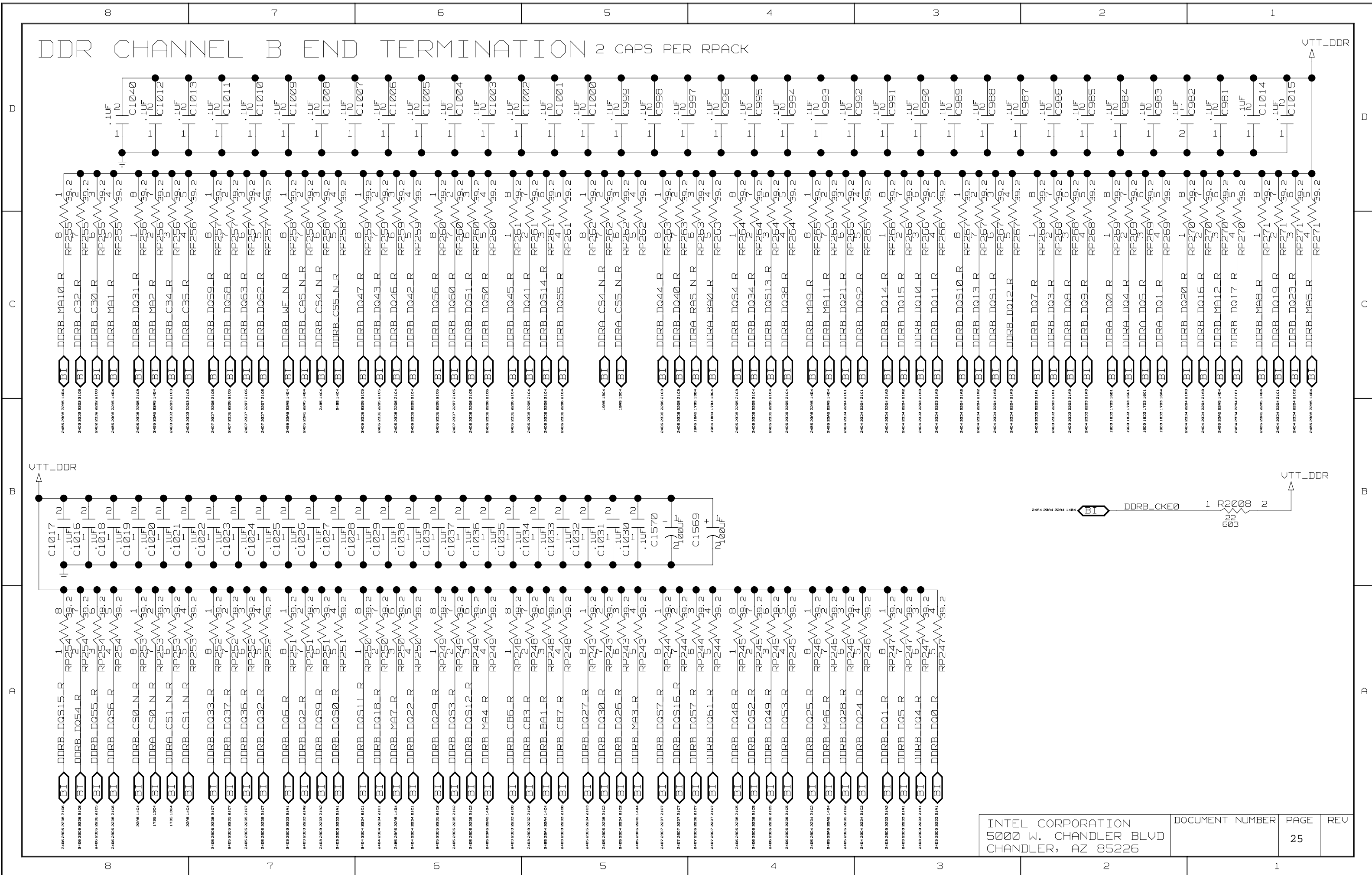
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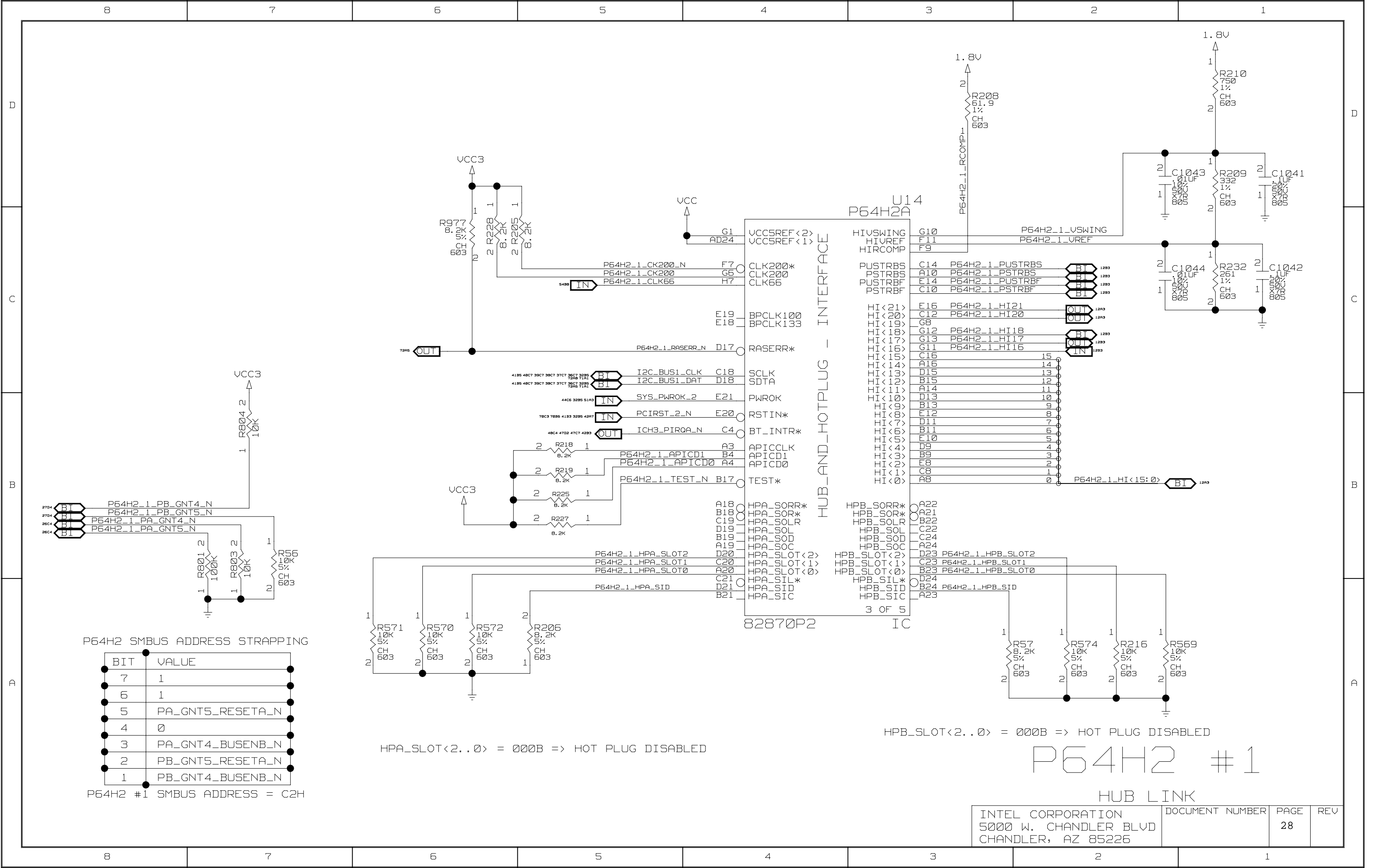
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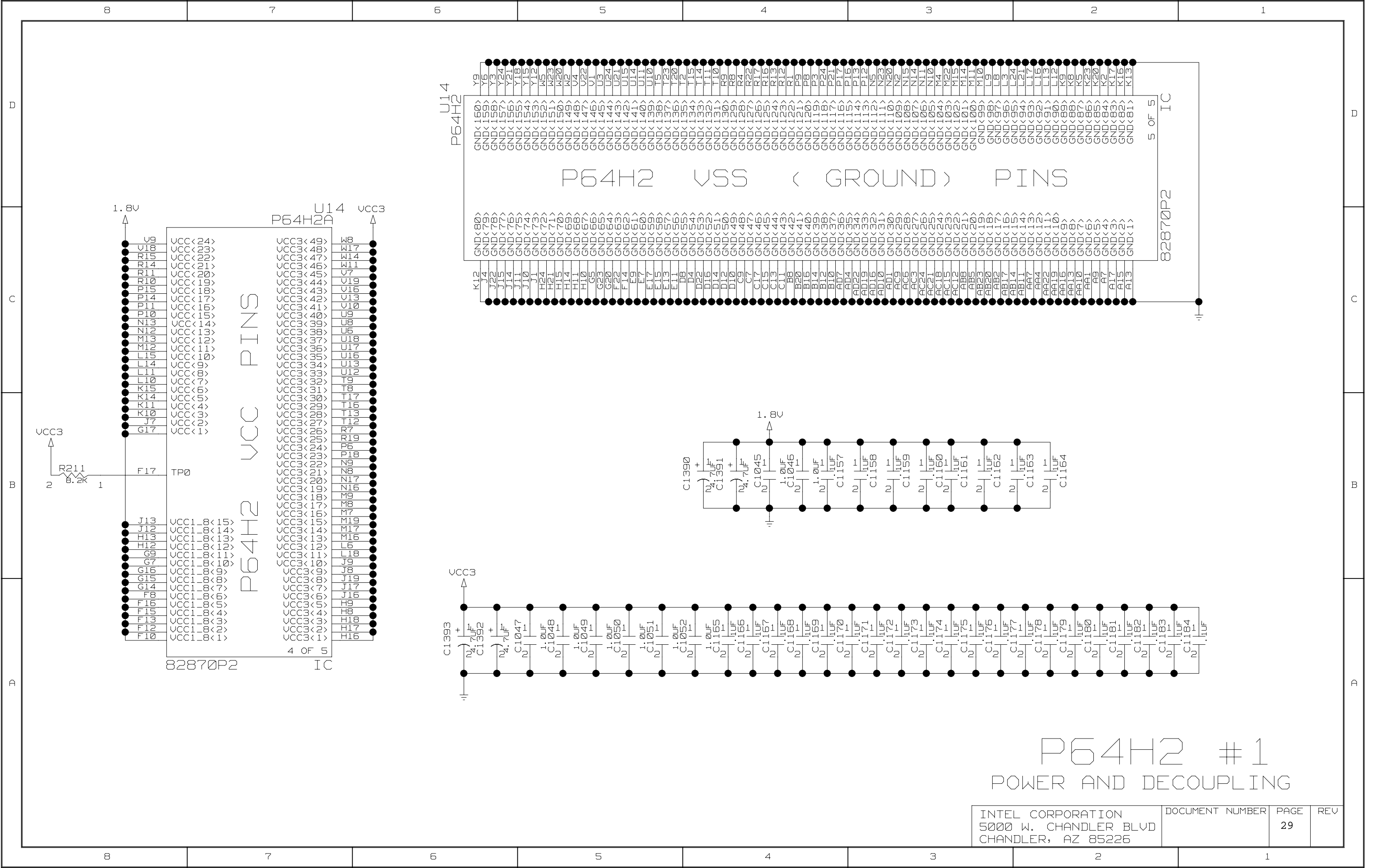
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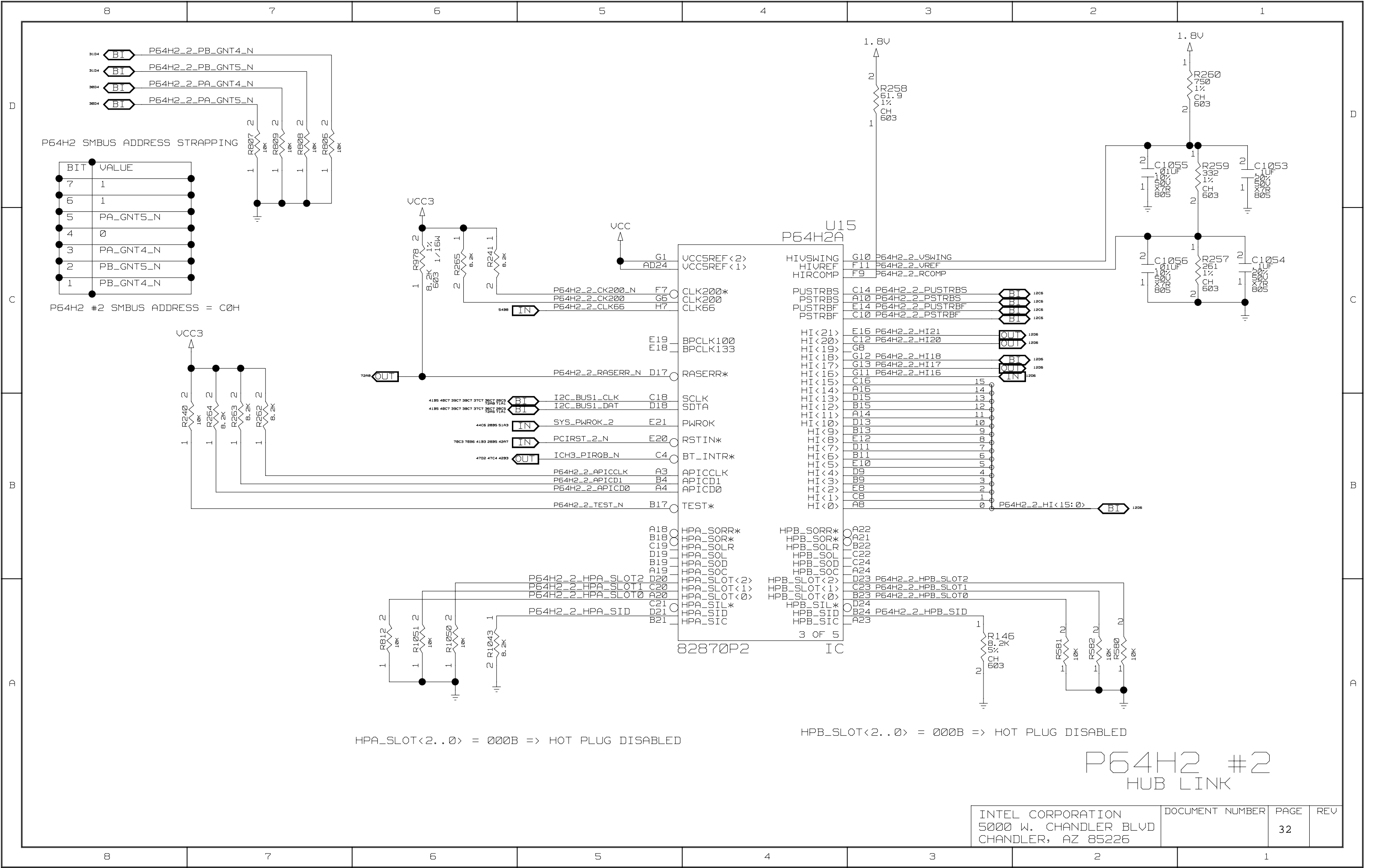
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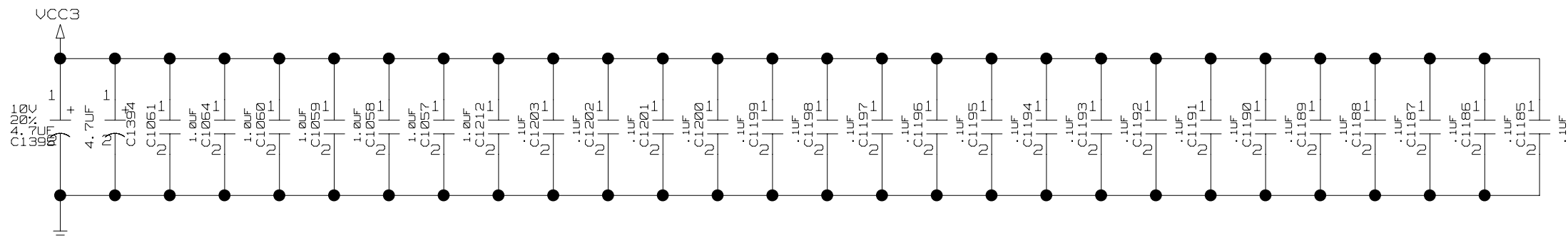
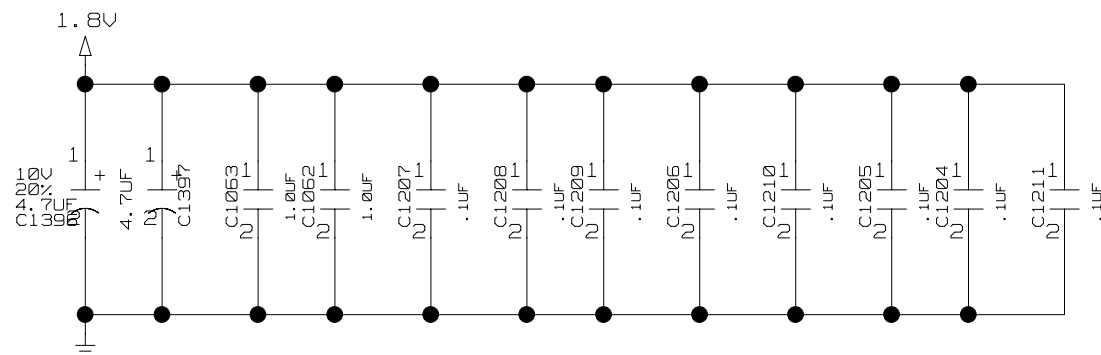
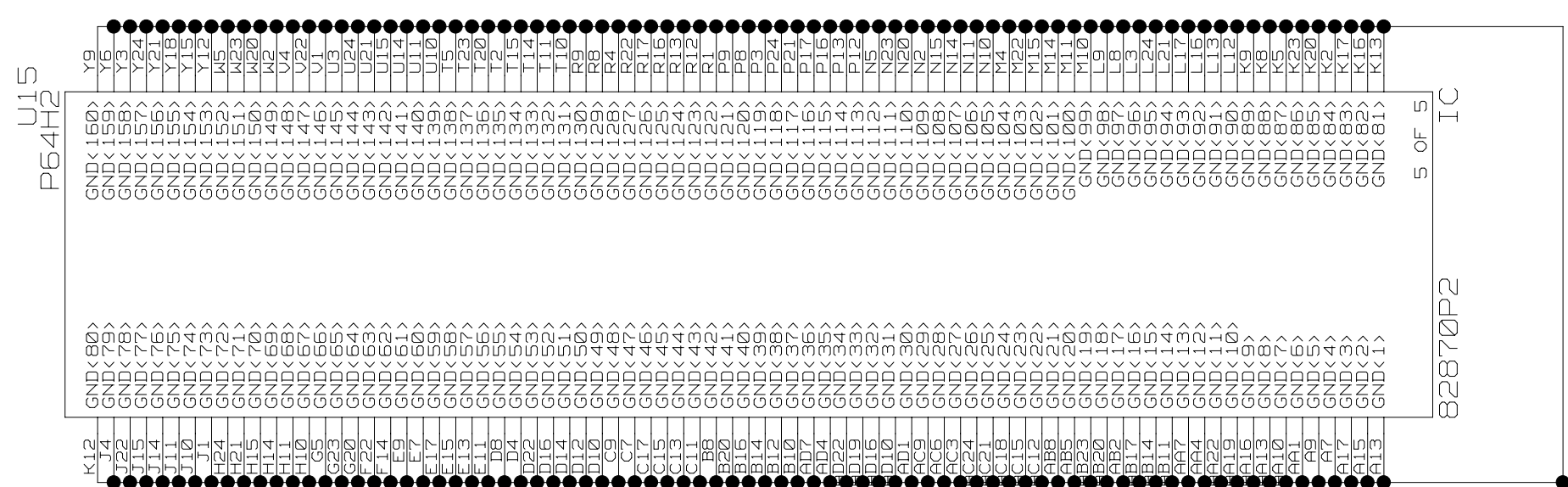
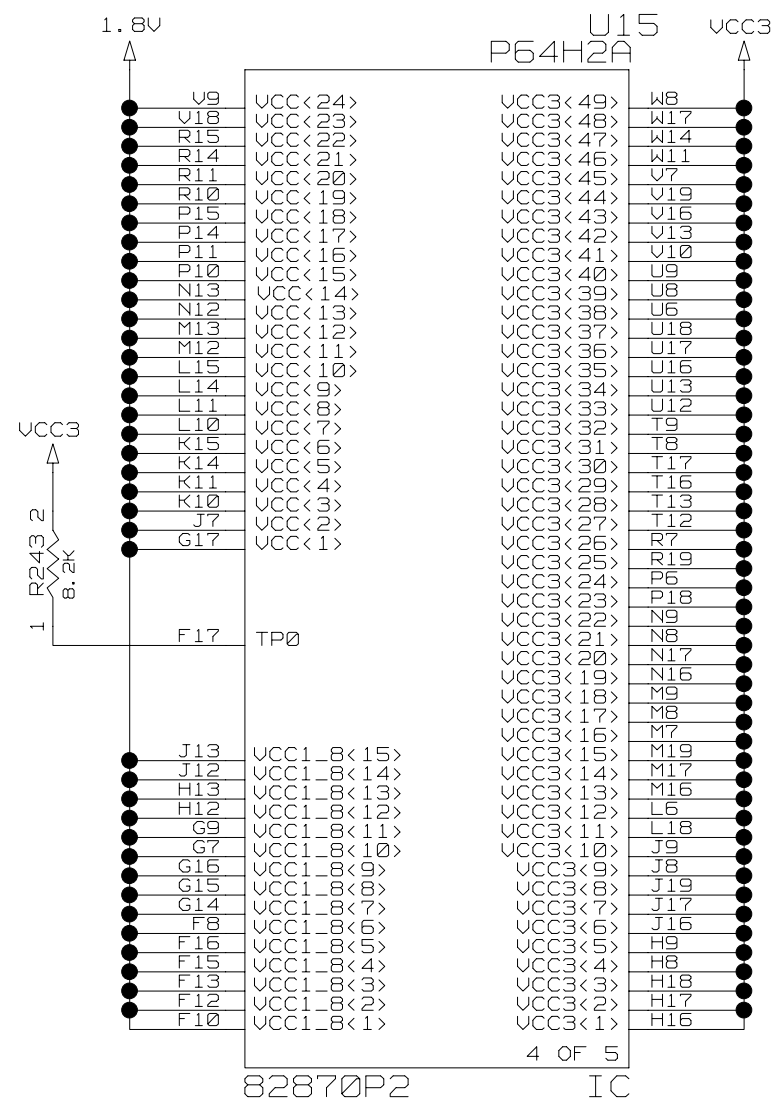












P64H2 #2

POWER AND DECOUPLING

P64H2 #1 PCI BUS A PULL-UPS

P64H2 #1 PCI BUS B PULL-UPS

D

C

B

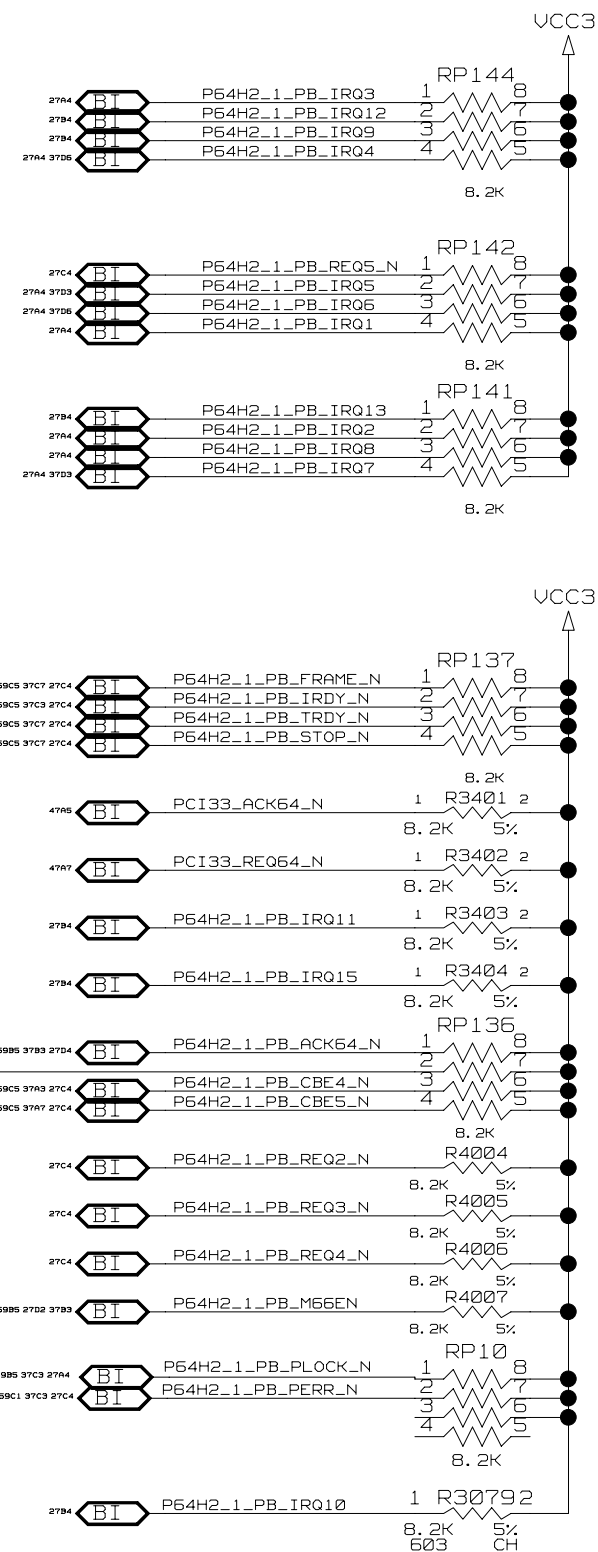
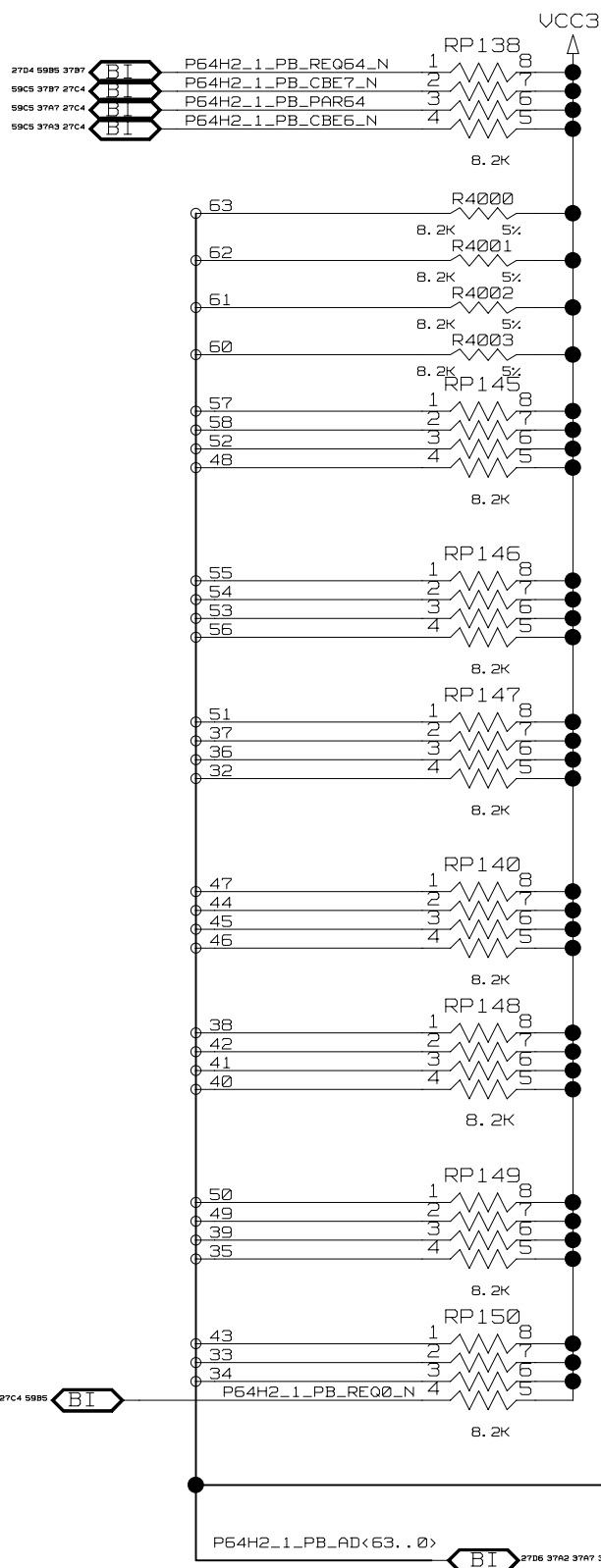
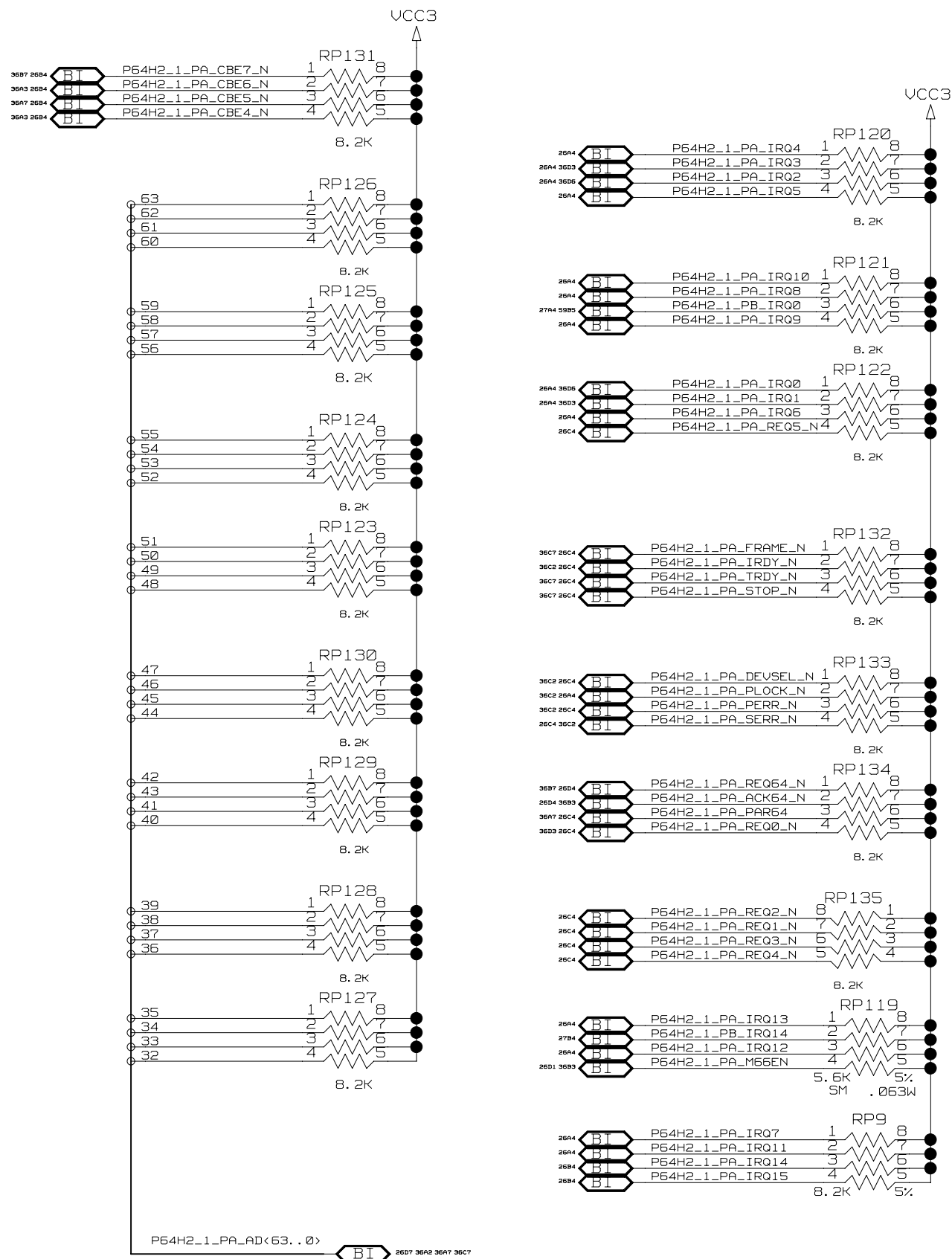
A

D

C

B

A



P64H2 #1 PCI PULL-UPS

P64H2 #2 PCI BUS A PULL-UPS

P64H2 #2 PCI BUS B PULL-UPS

D

C

B

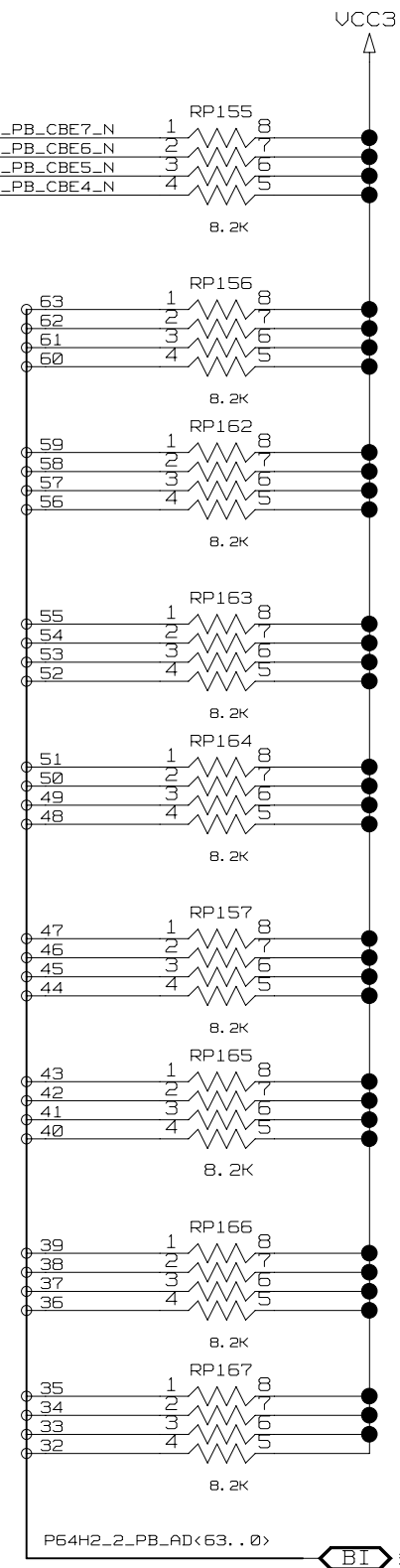
A

D

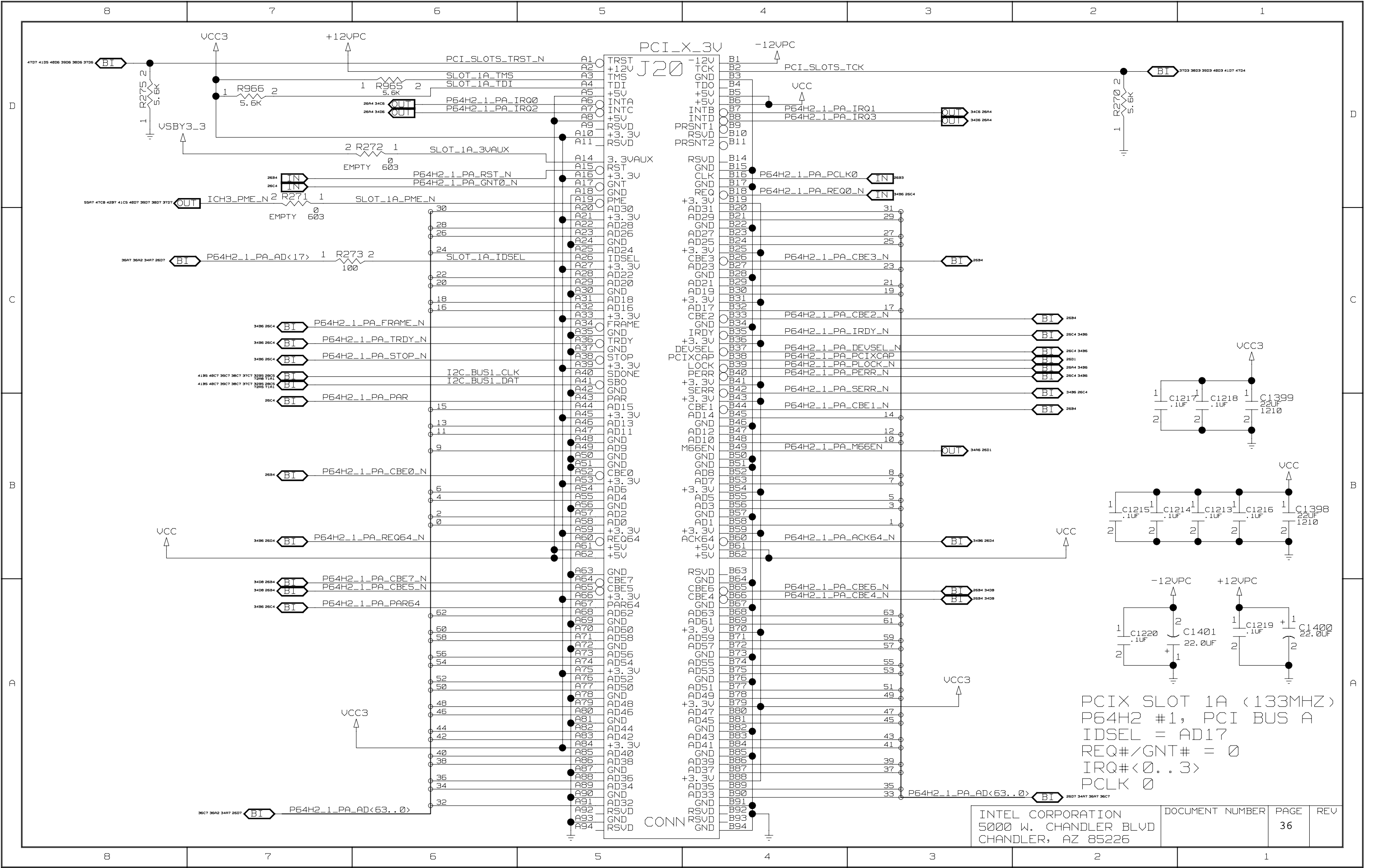
C

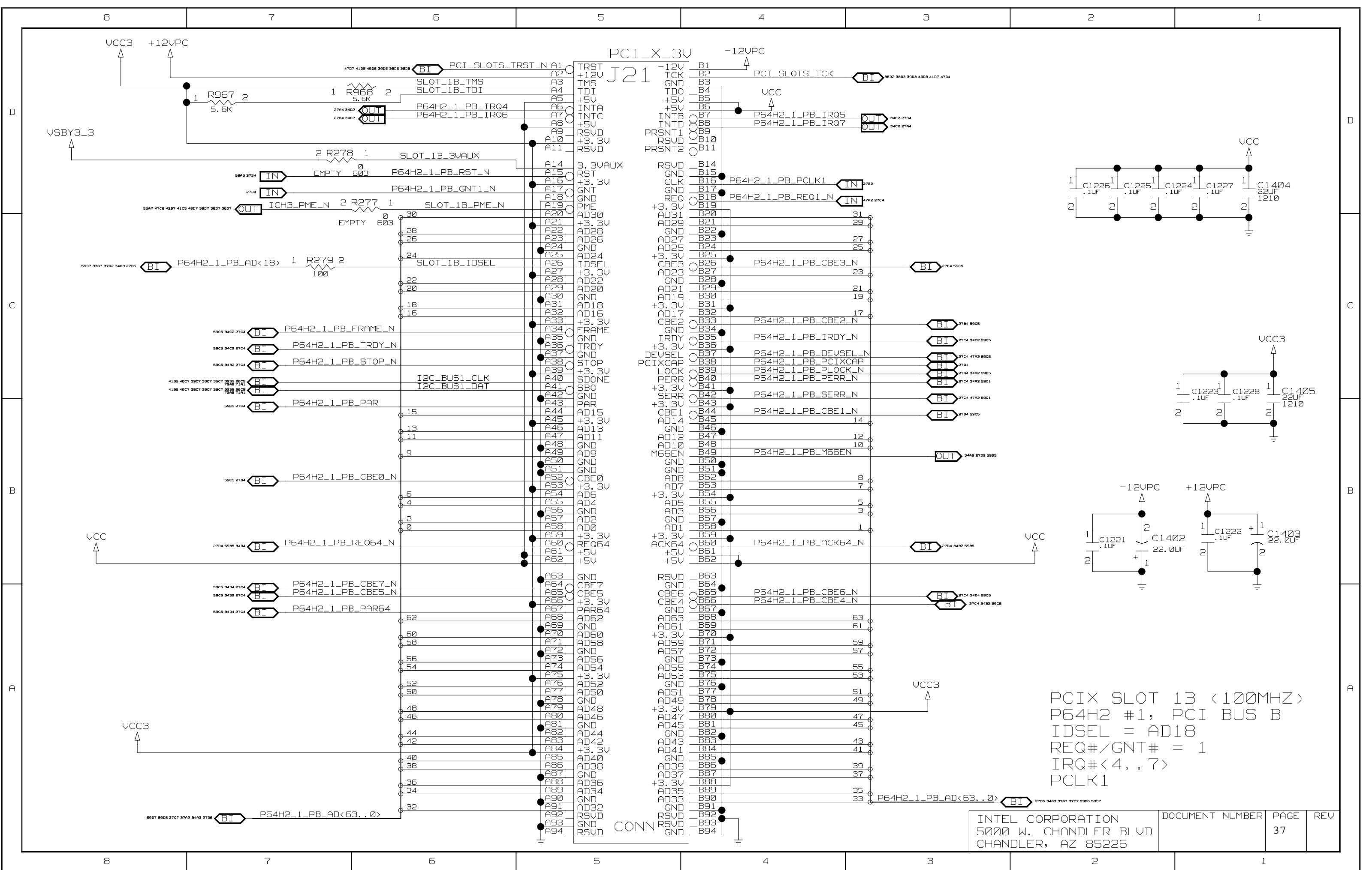
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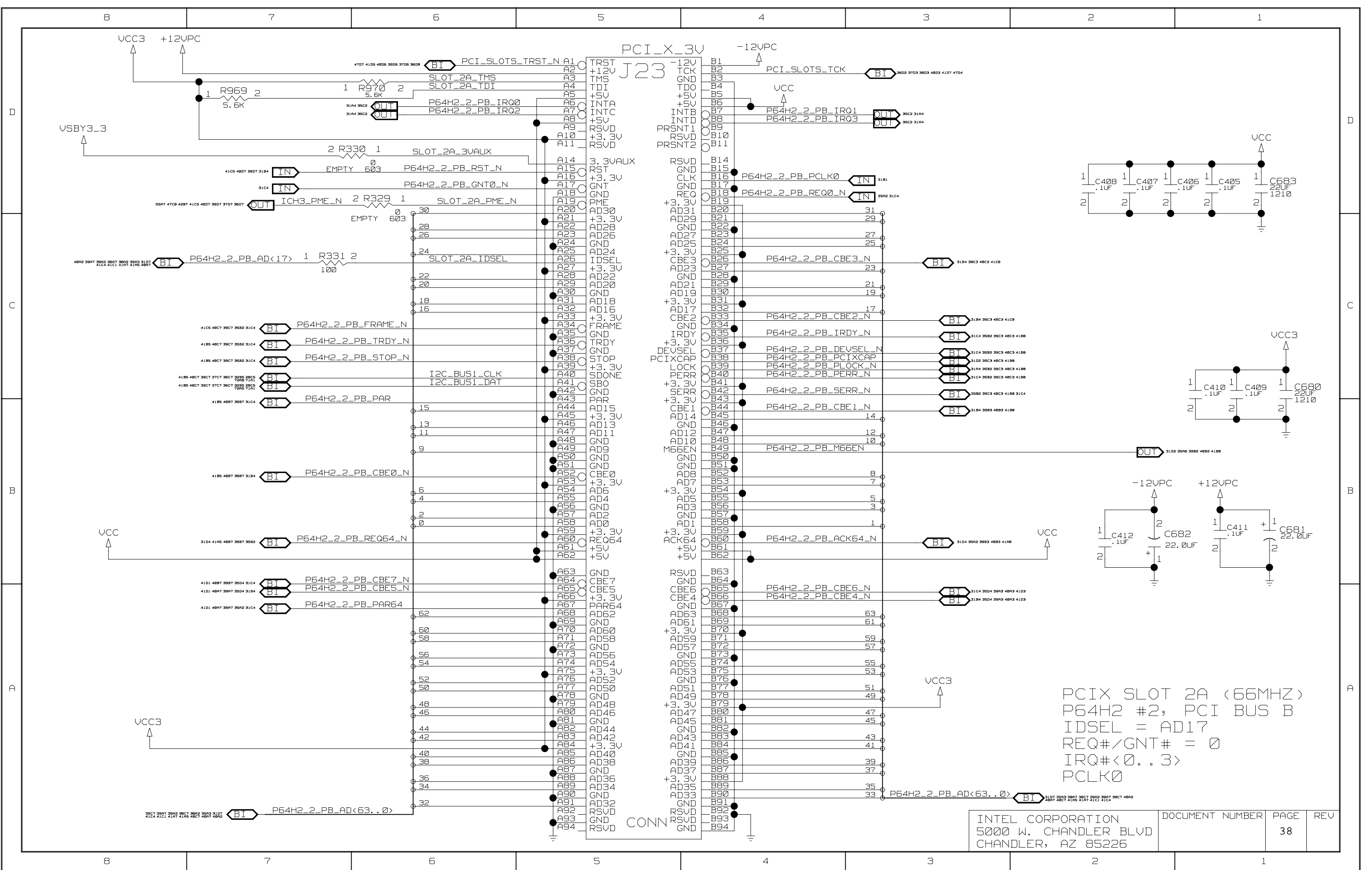
A

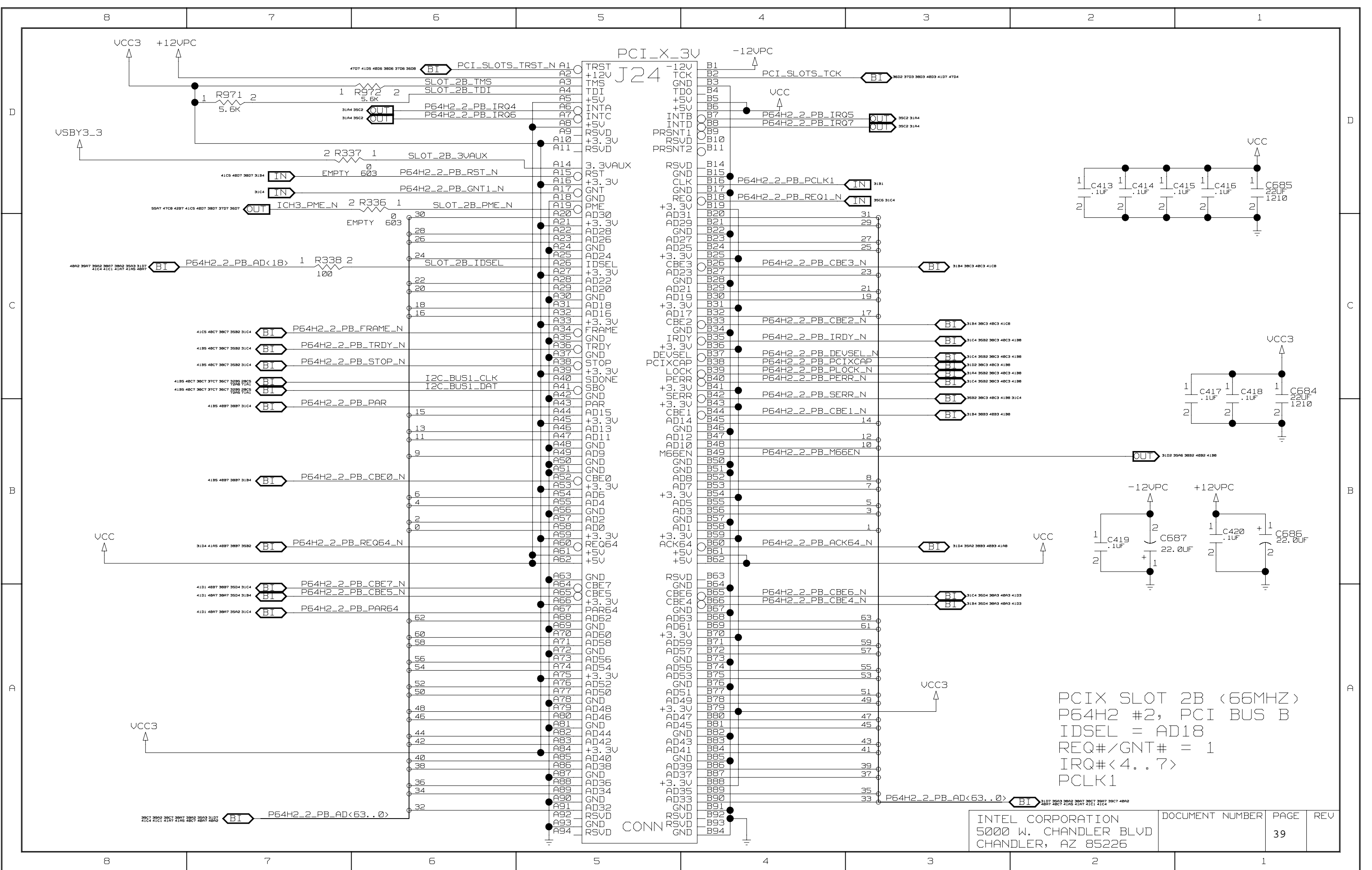


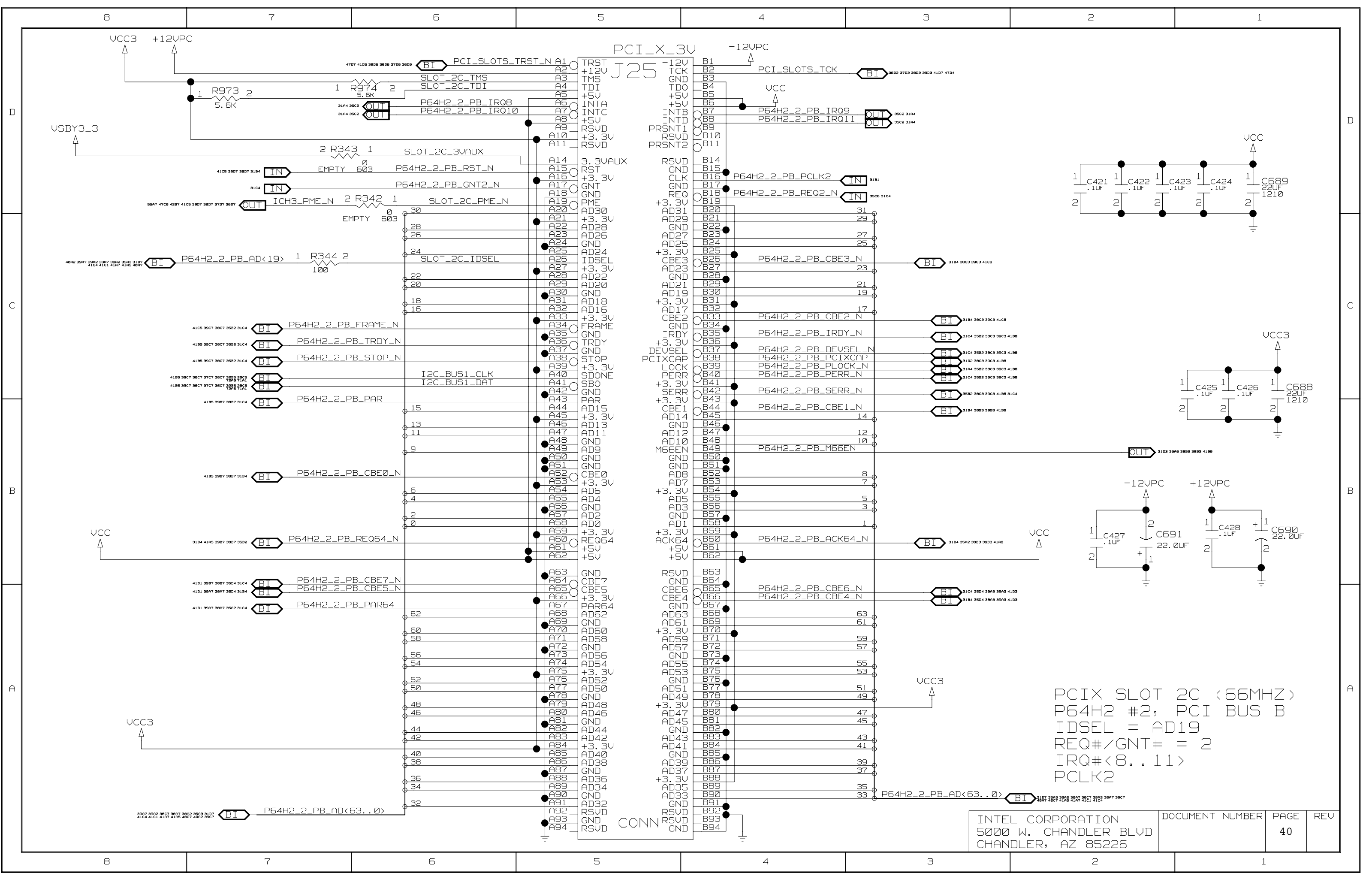
P64H2 #2 PCI PULL-UPS



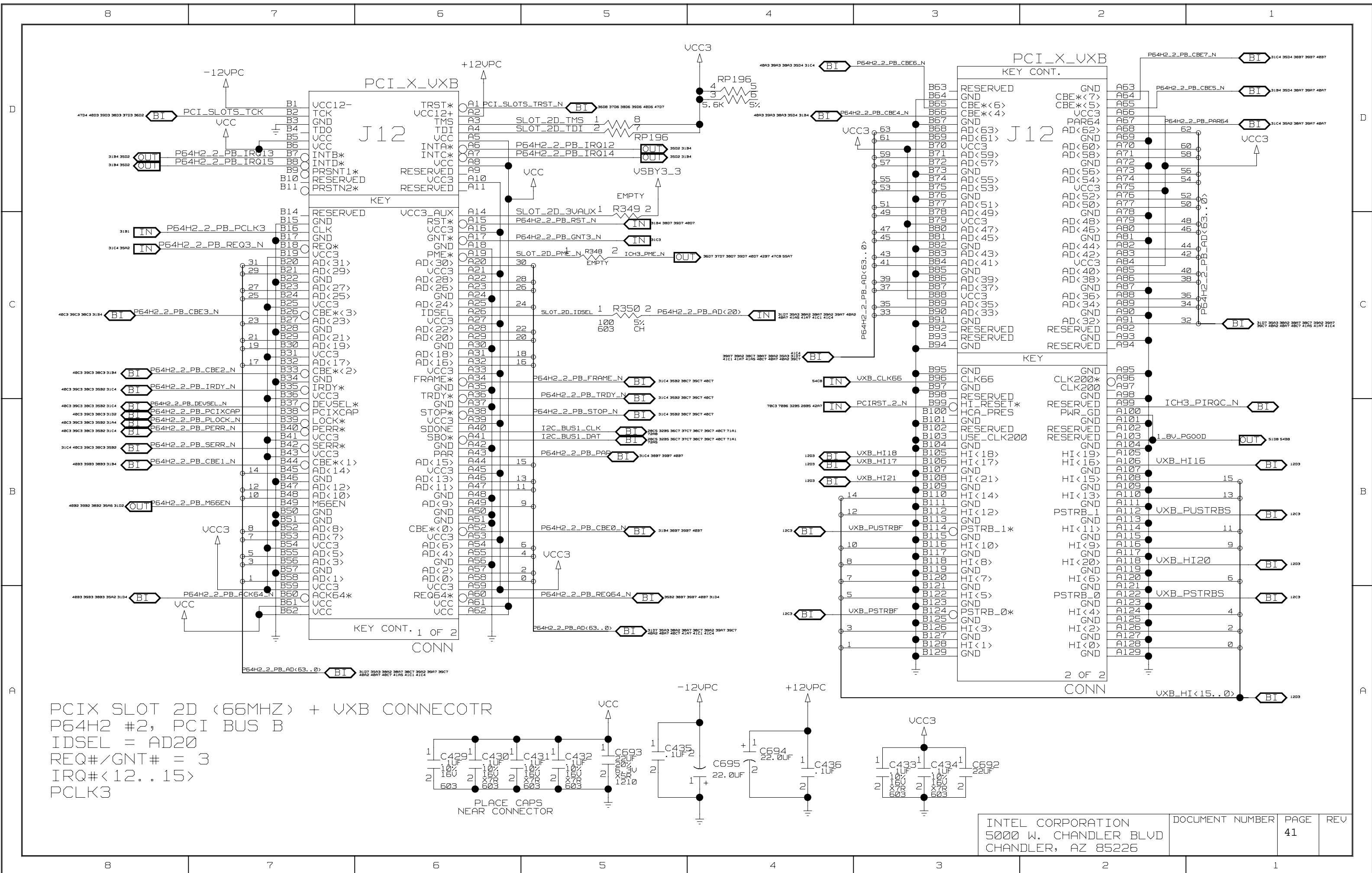




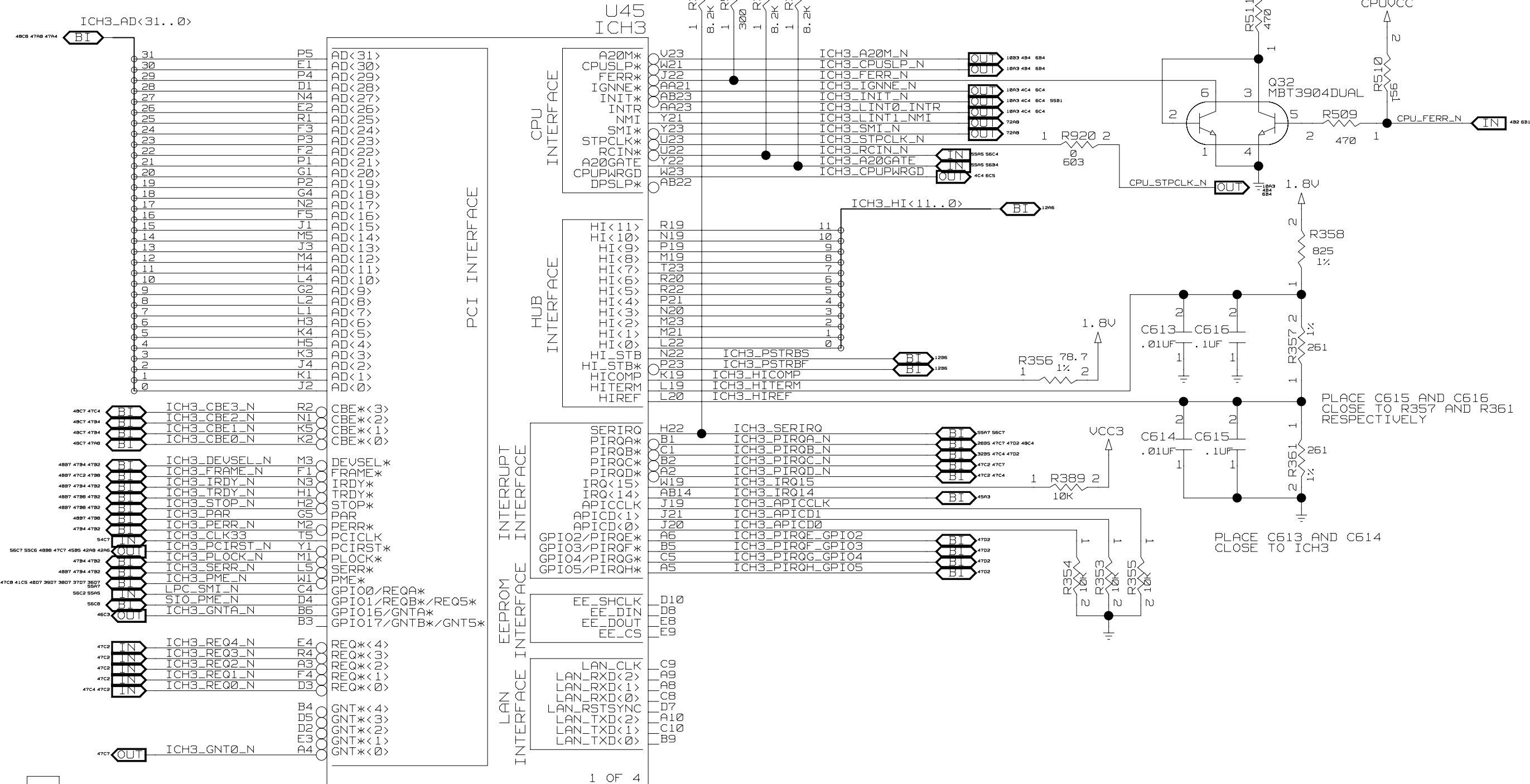




PCIX SLOT 2C (66MHZ)
P64H2 #2, PCI BUS B
IDSEL = AD19
REQ#/GNT# = 2
IRQ#<8..11>
PCLK2



ICH3 (PART 1 OF 4)



D

C

B

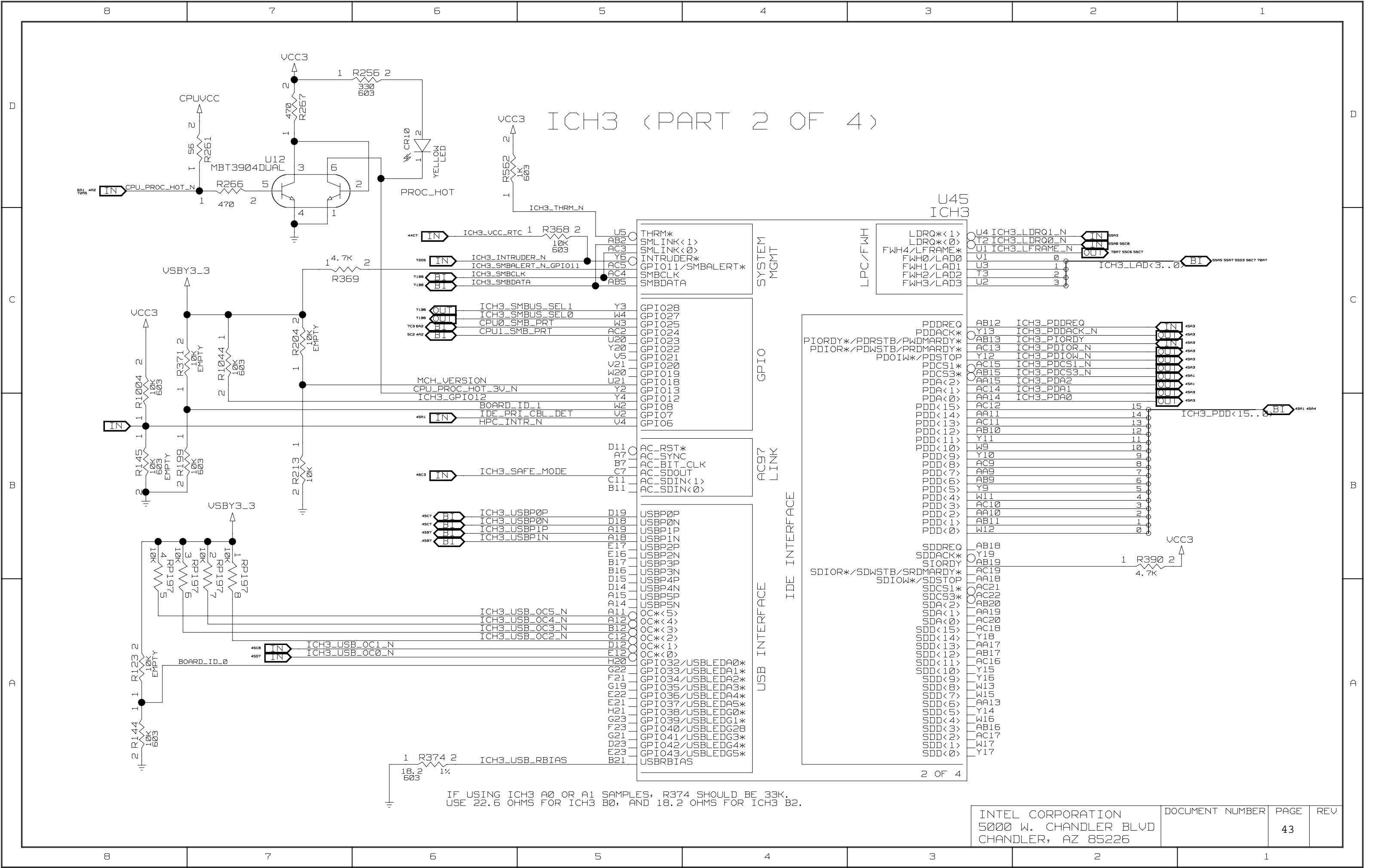
A

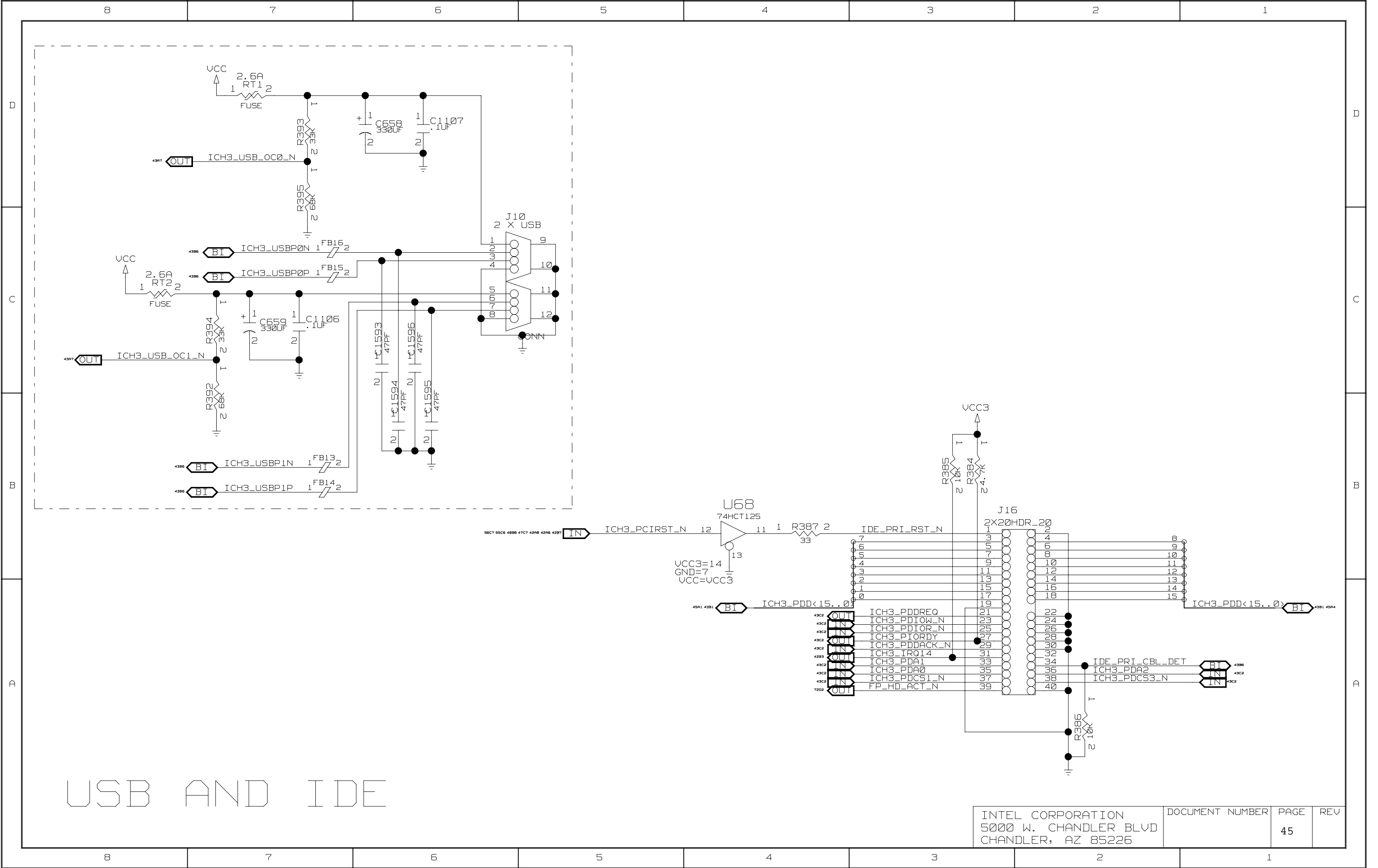
D

C

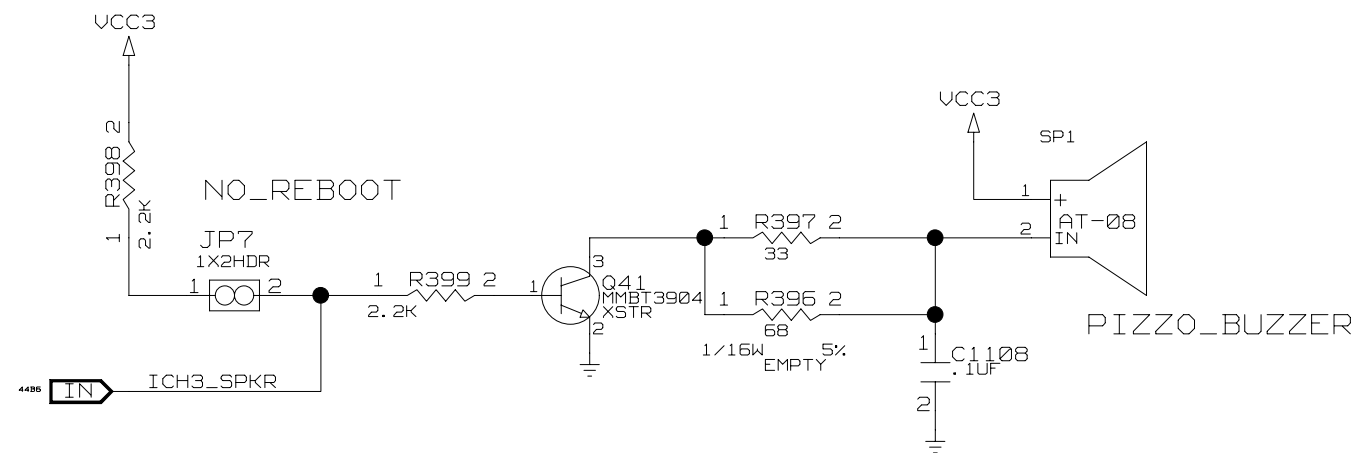
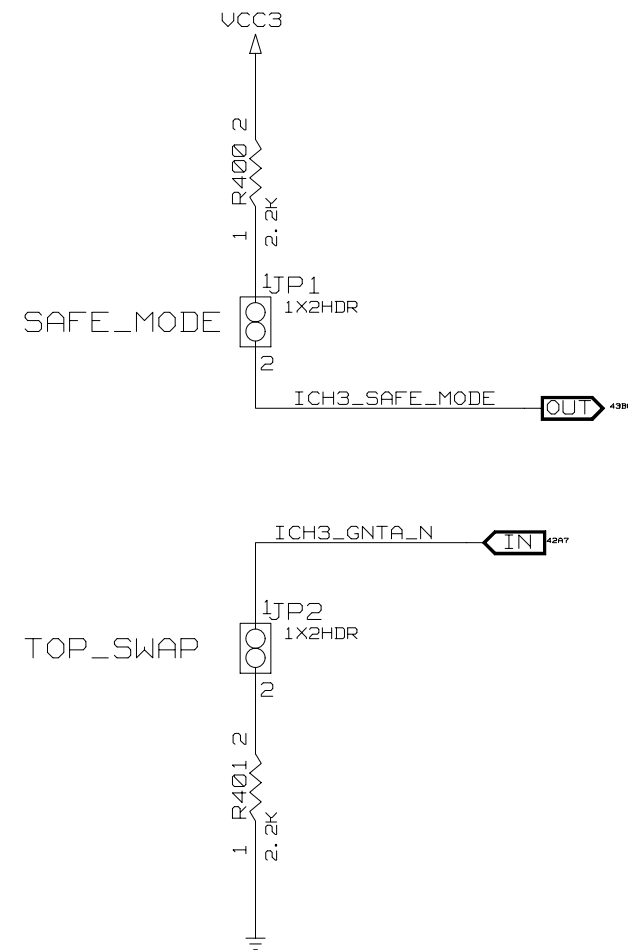
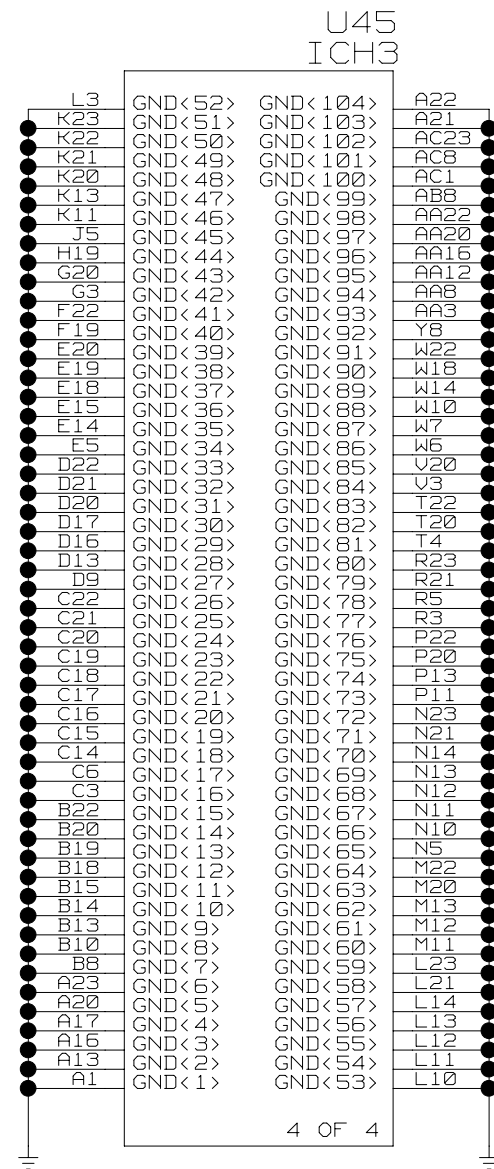
B

A



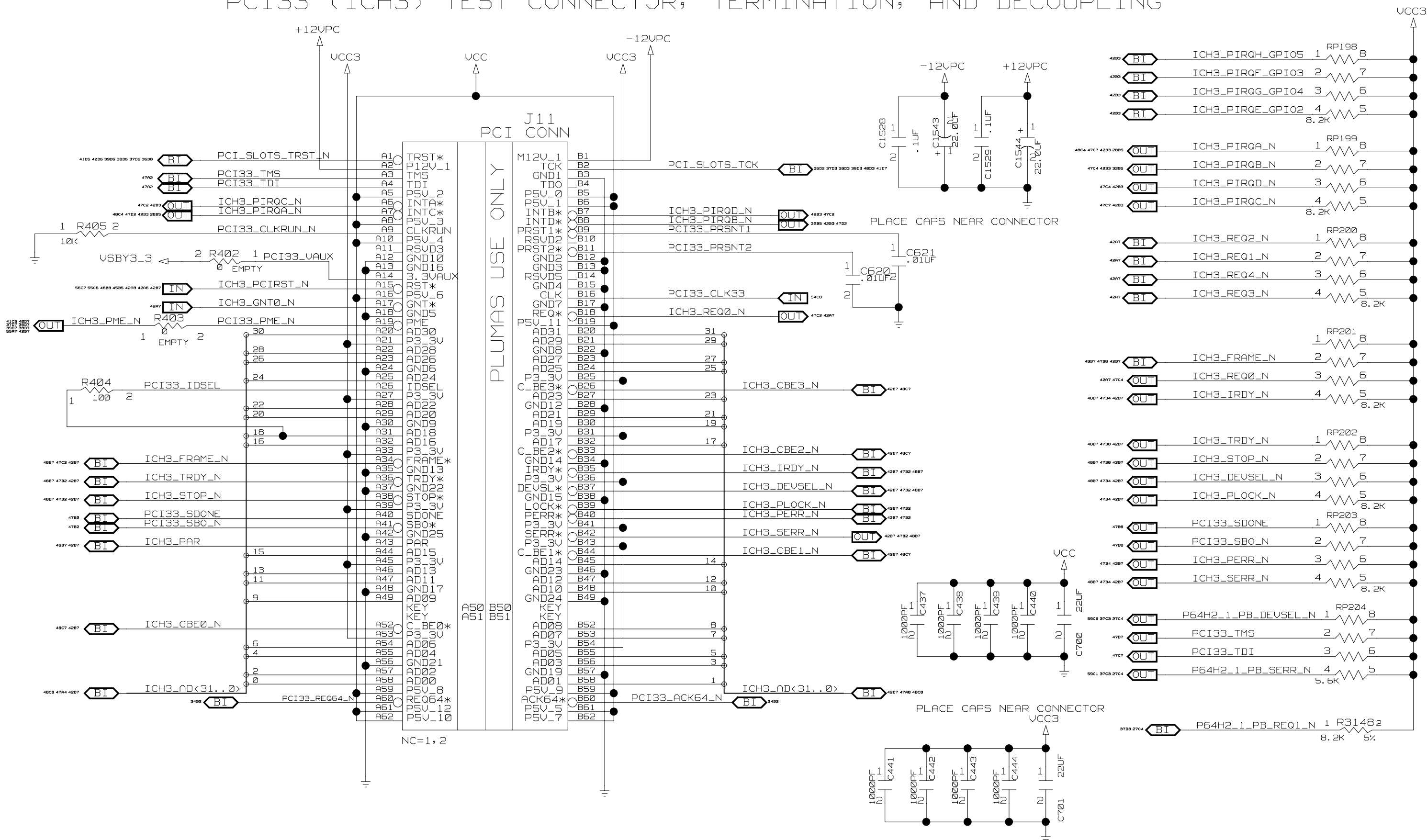


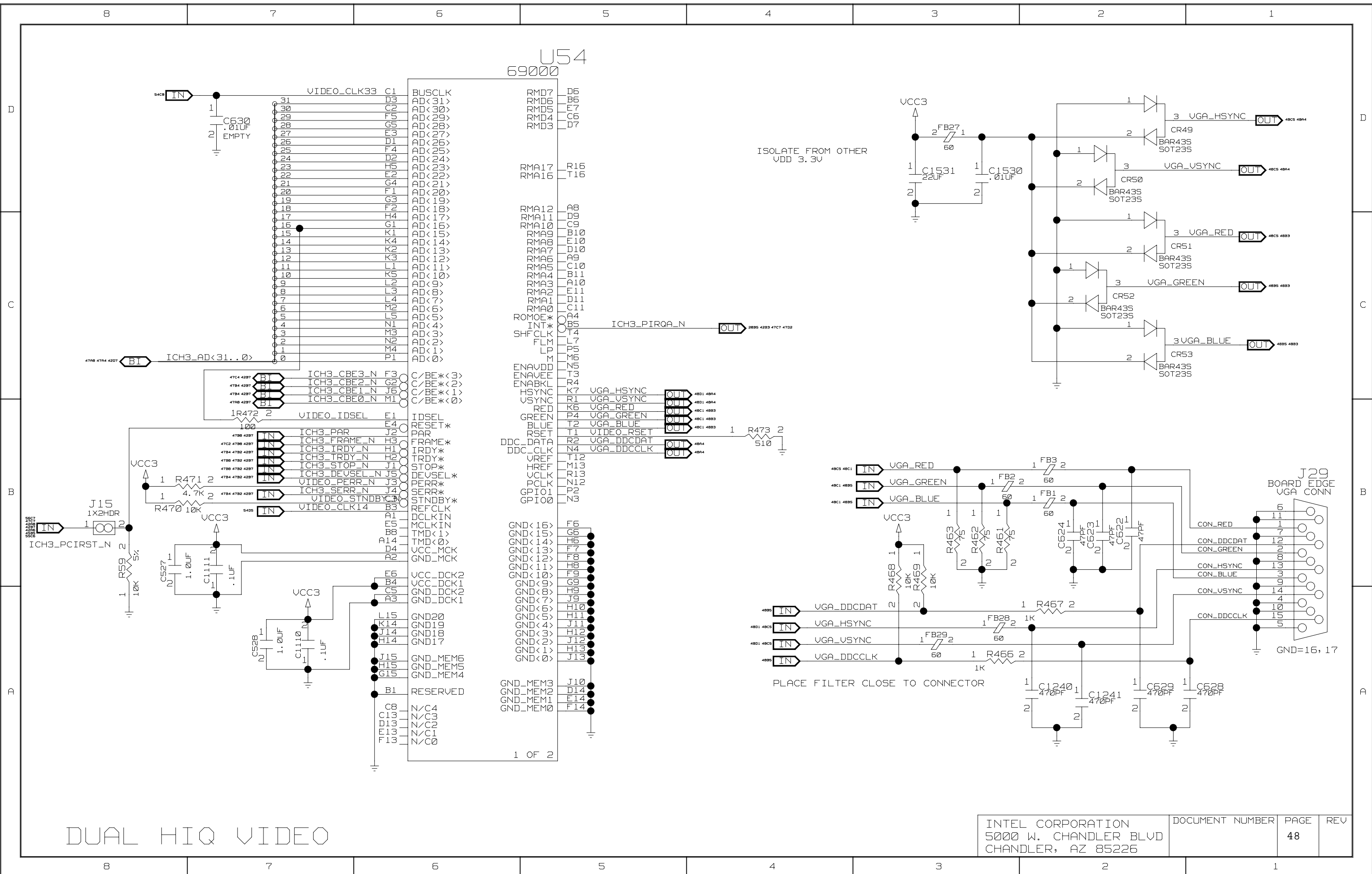
ICH3 (PART 4 OF 4)

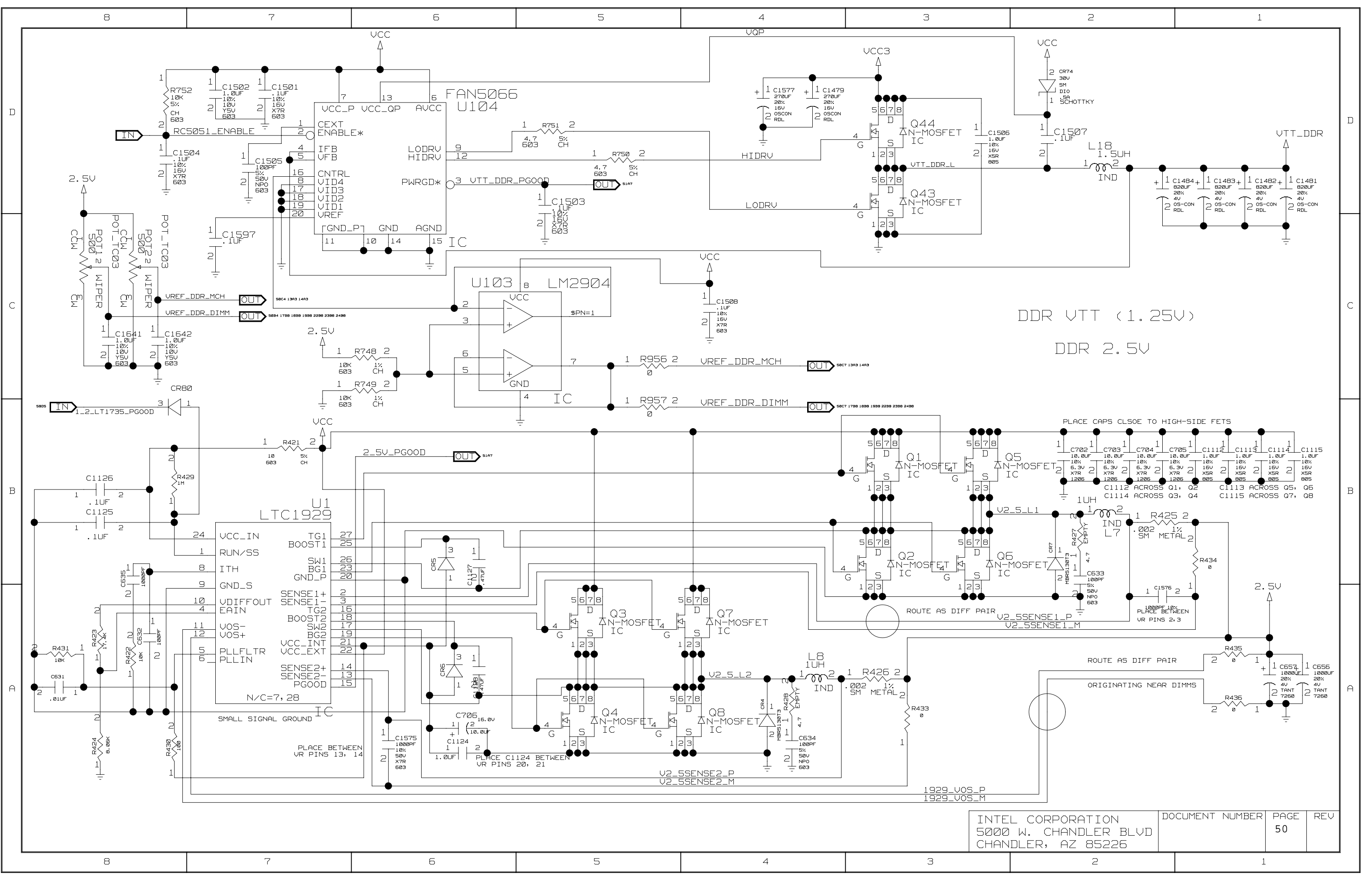


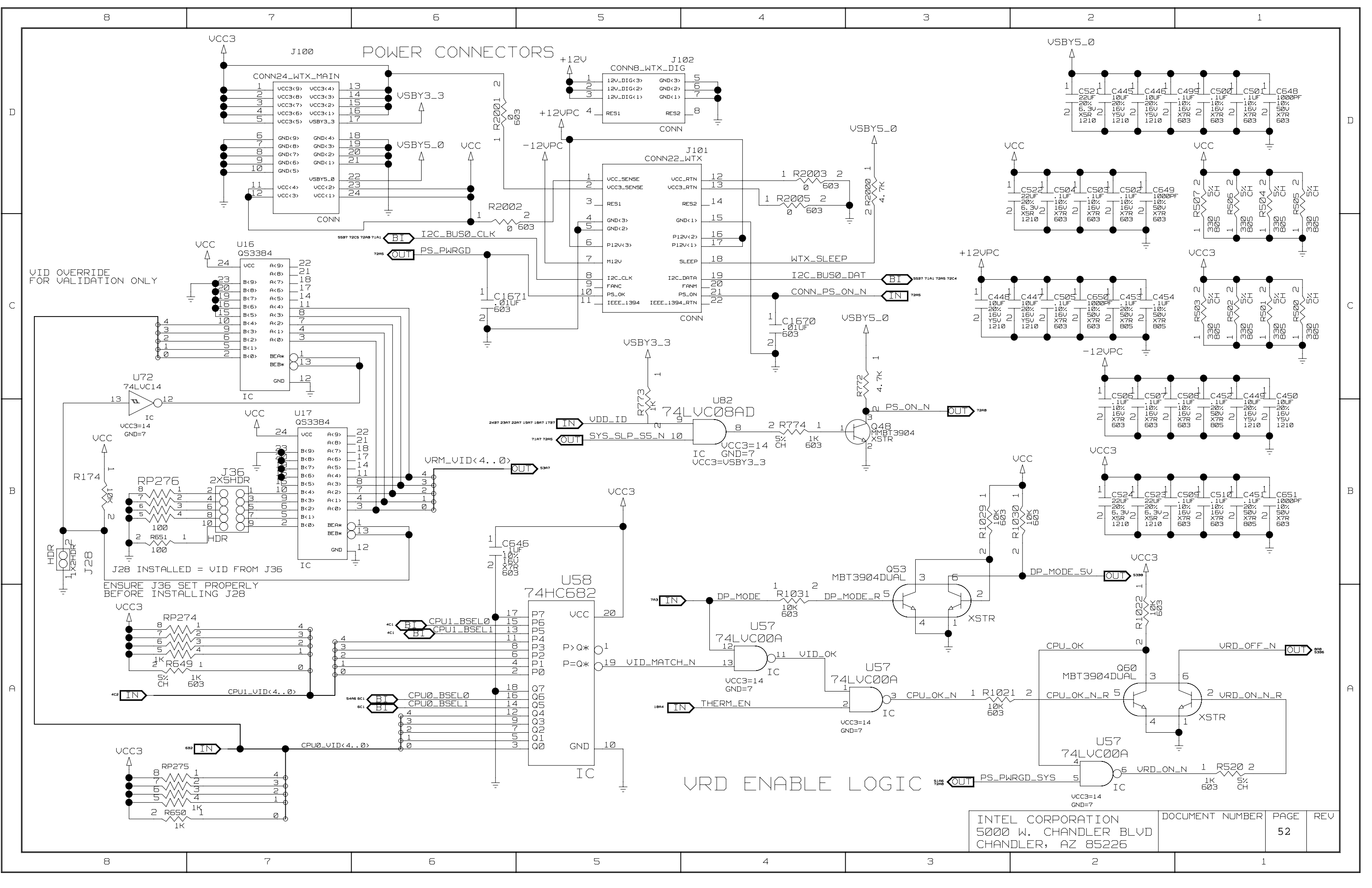
STRAP OPTIONS AND SPEAKER CIRCUITRY

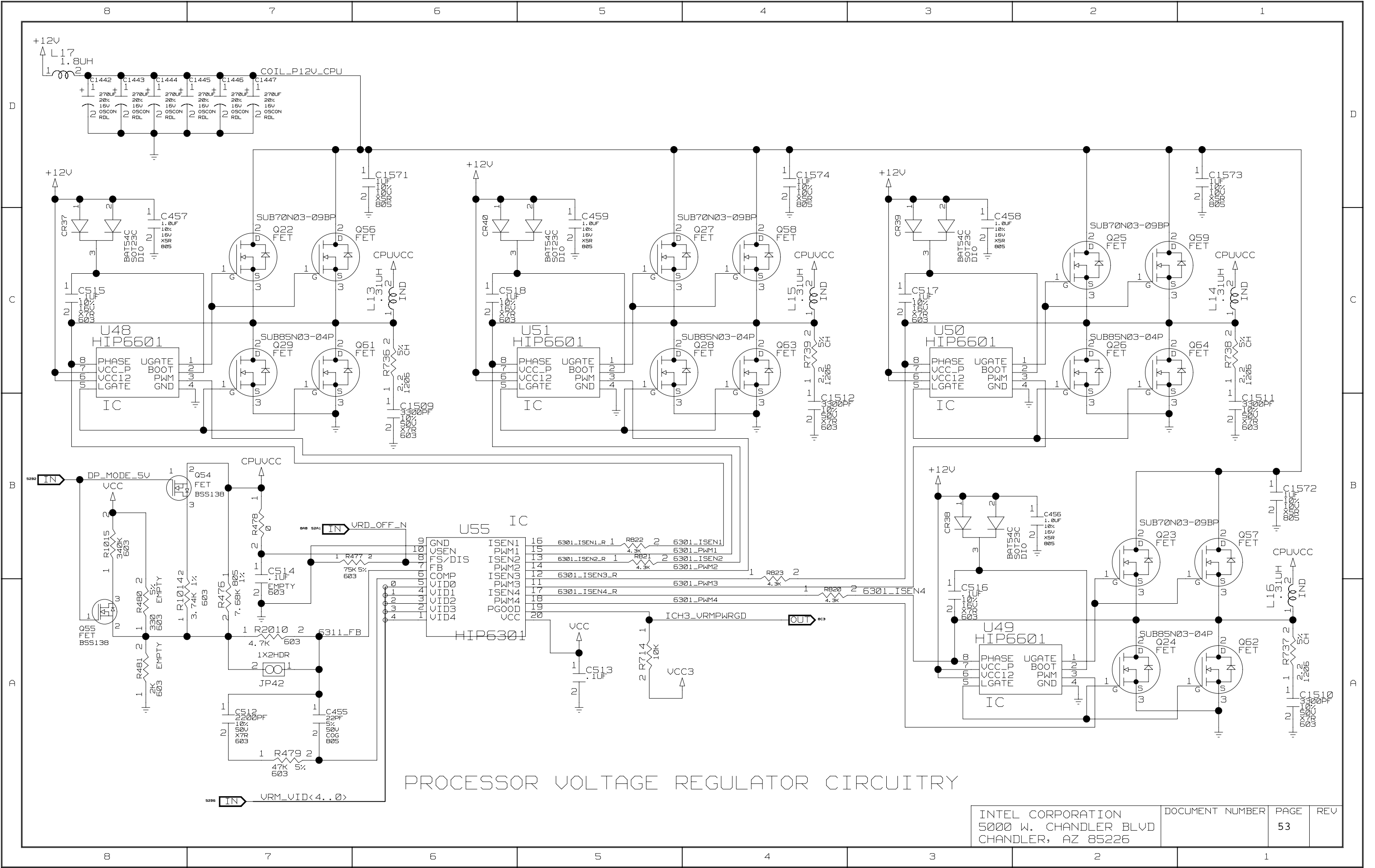
PCI33 (ICH3) TEST CONNECTOR, TERMINATION, AND DECOUPLING

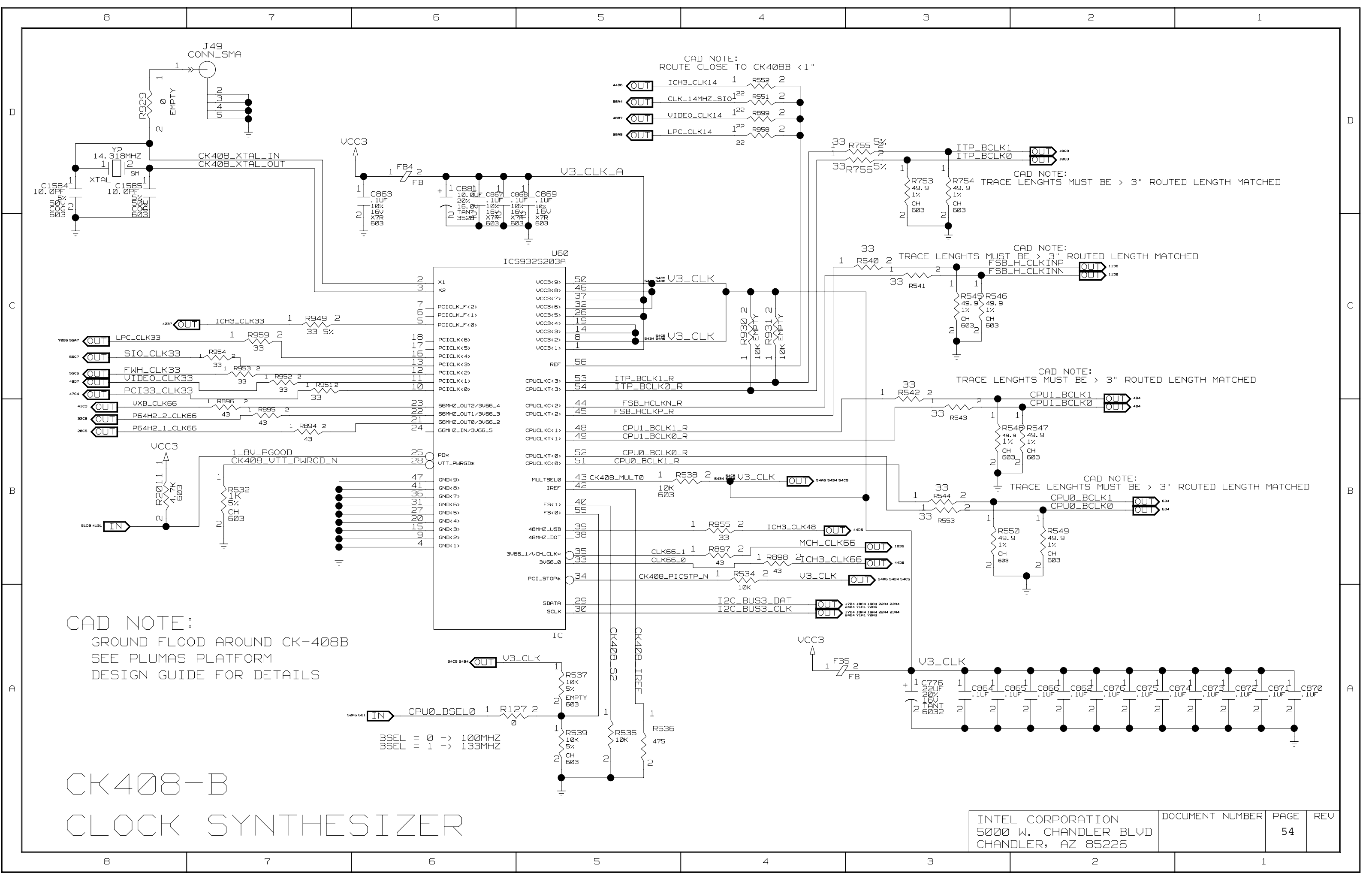








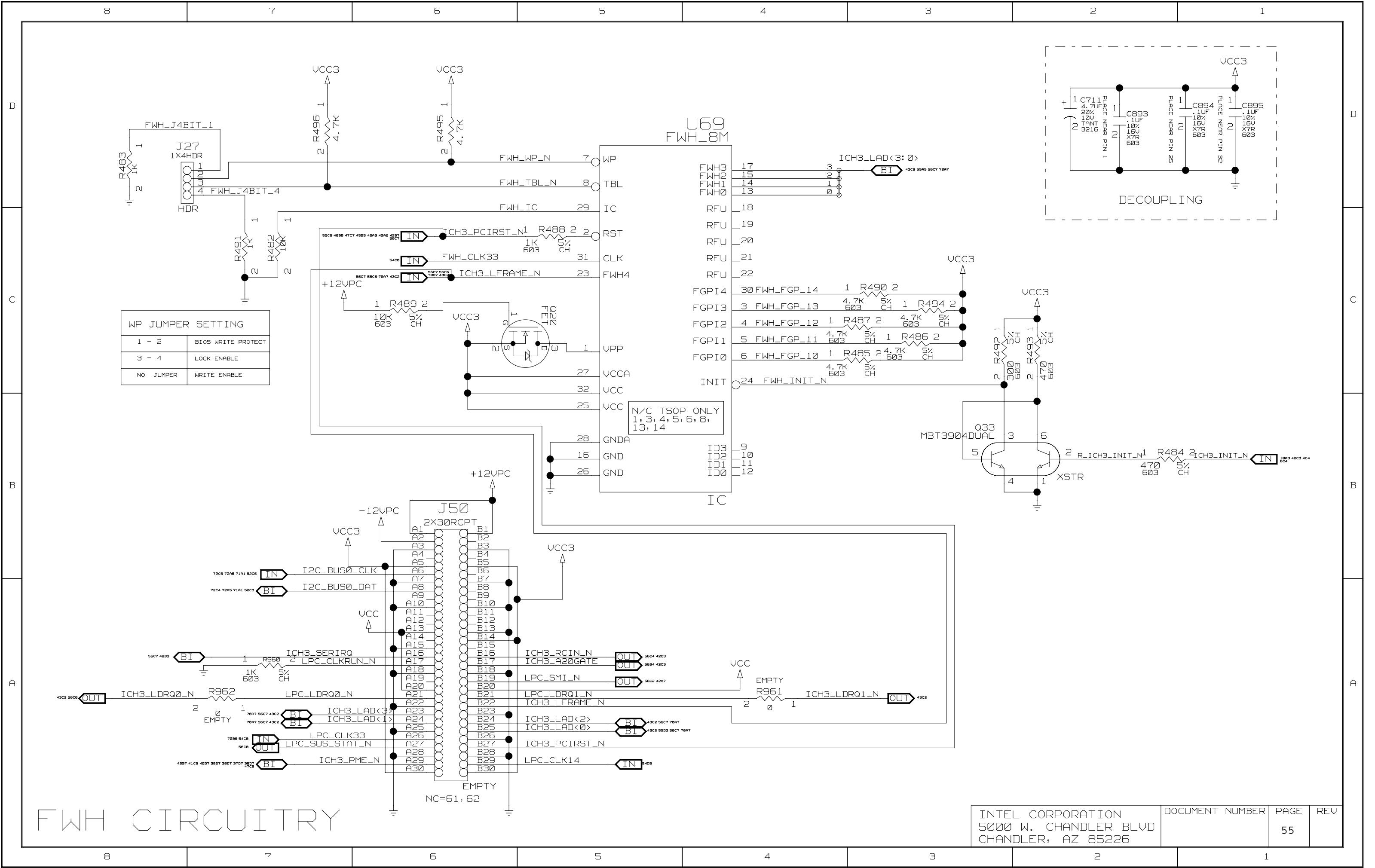




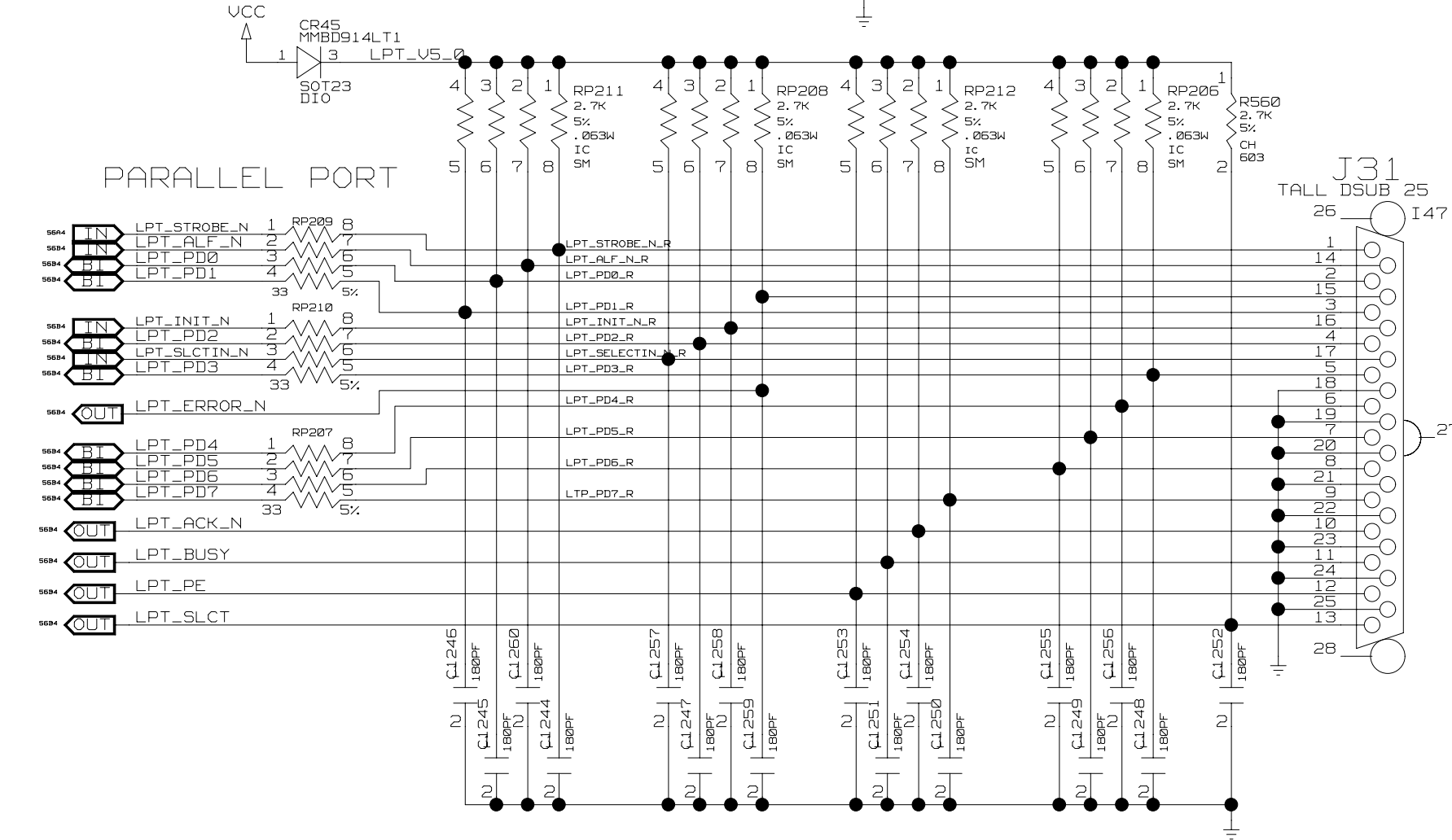
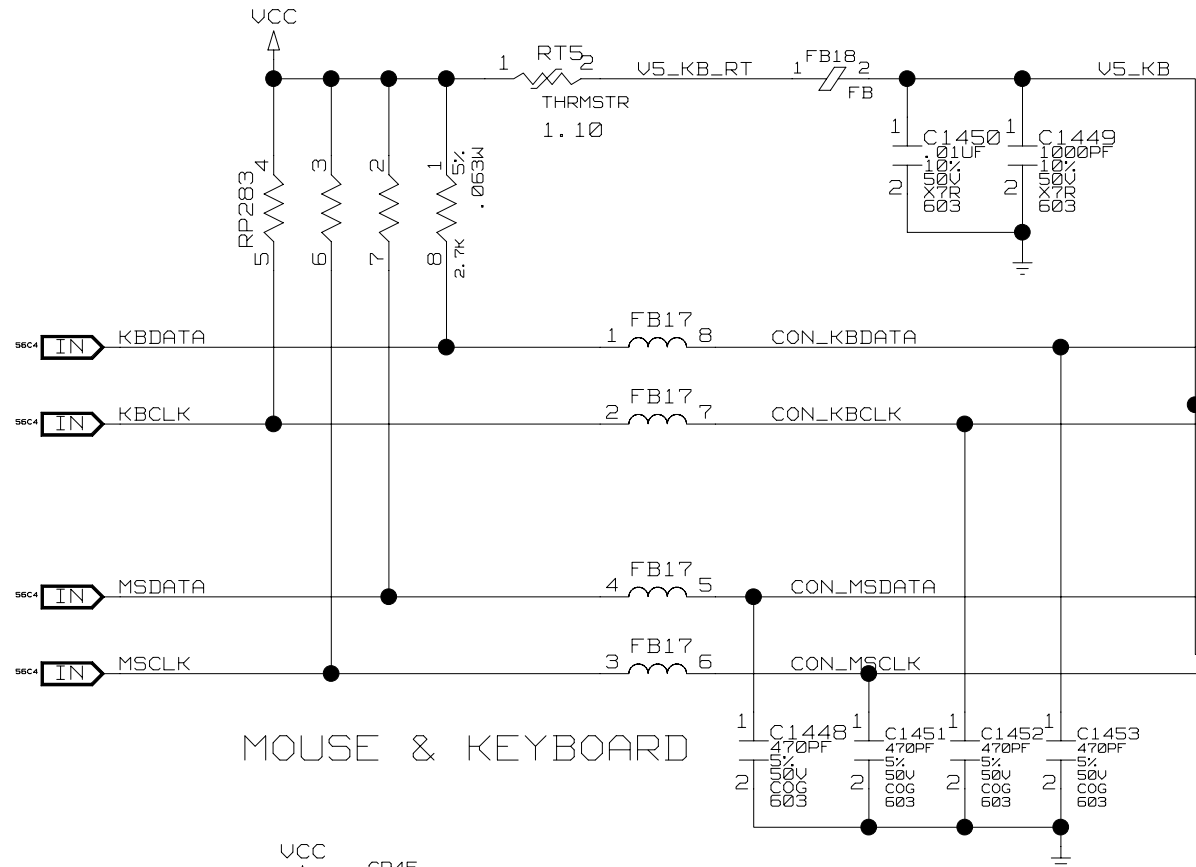
CAD NOTE:
GROUND FLOOD AROUND CK-408B
SEE PLUMAS PLATFORM
DESIGN GUIDE FOR DETAILS

CK408-B CLOCK SYNTHESIZER

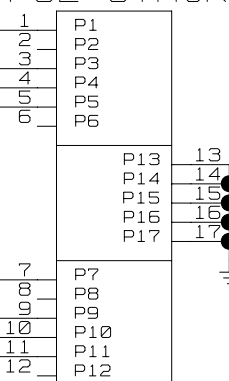
BSEL = 0 -> 100MHZ
BSEL = 1 -> 133MHZ



LEGACY I/O

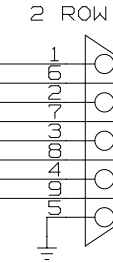


J40 PS2 STACK



KYBD AND MOUSE
SWAPPED TO PC STANDARD

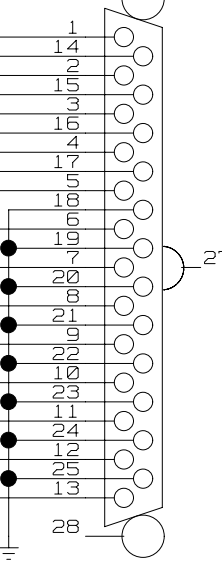
J35



SERIAL PORT

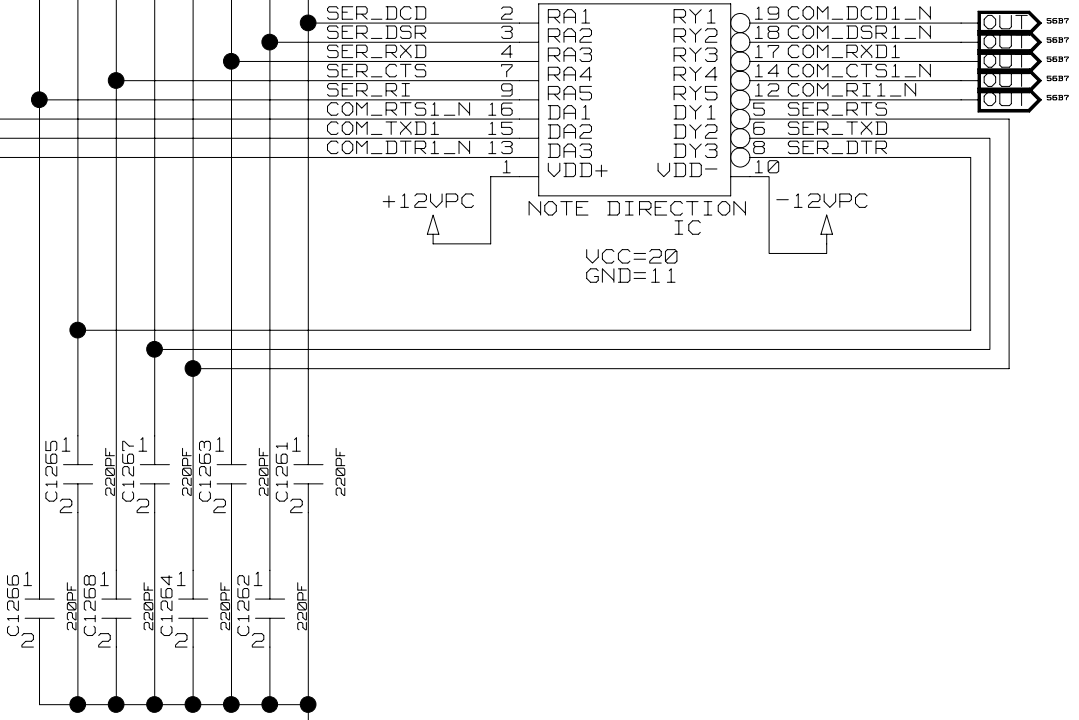


J31 TALL DSUB 25



U61

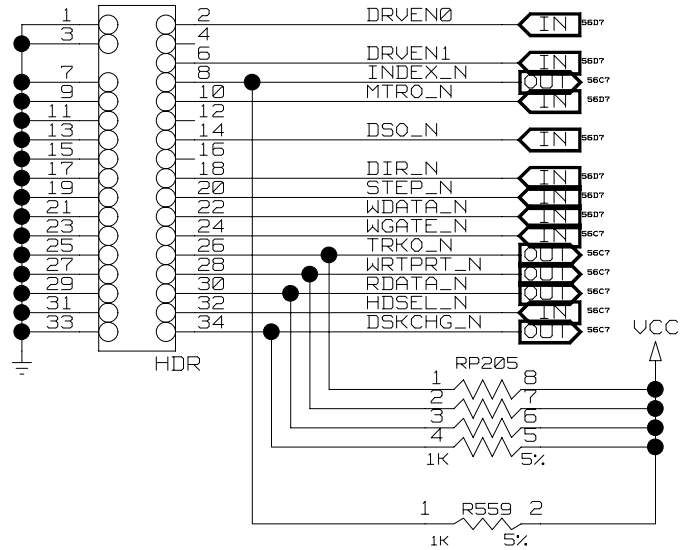
GD752325



FLOPPY CONNECTOR

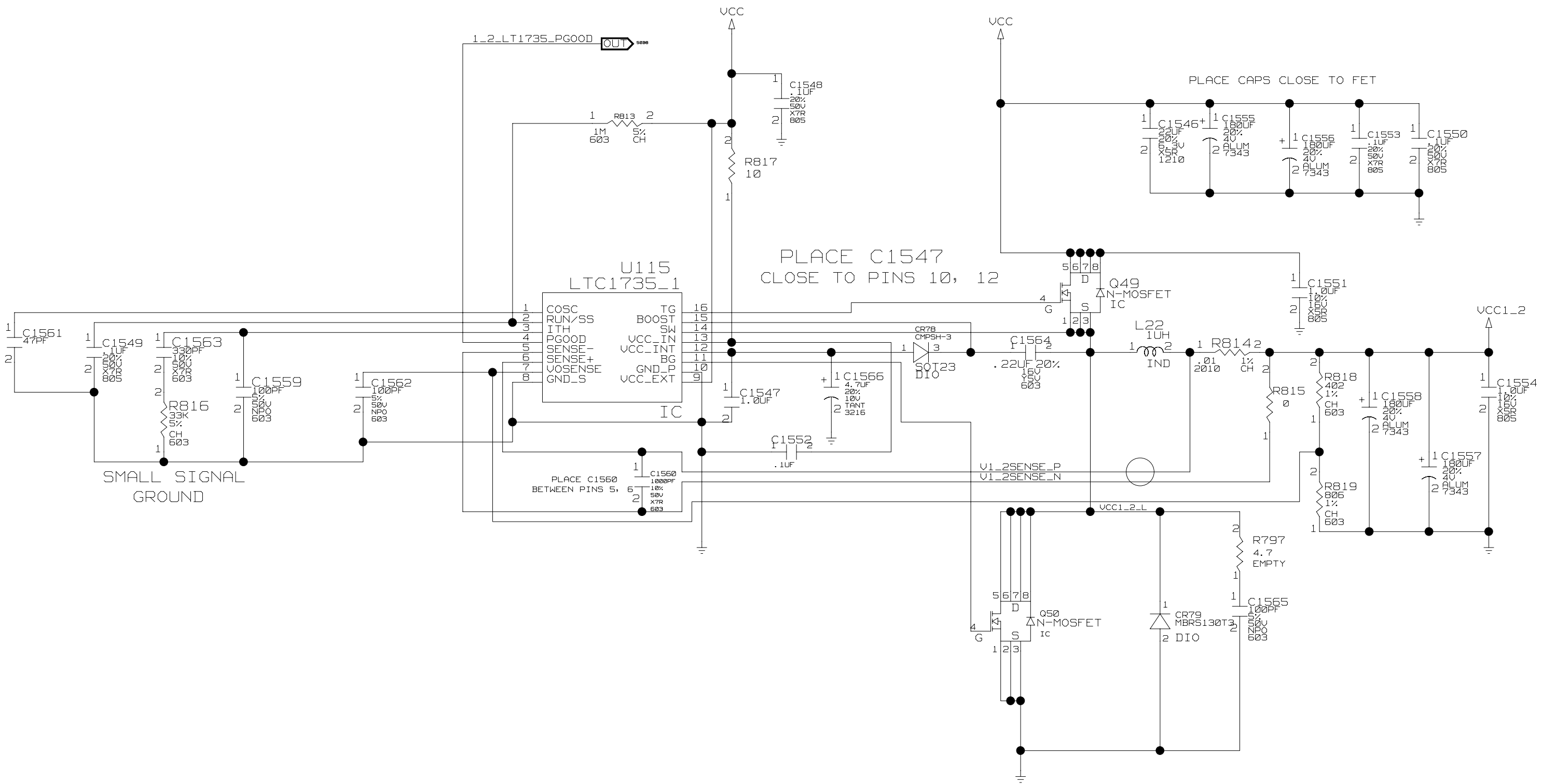
J34

2X17HDR_5

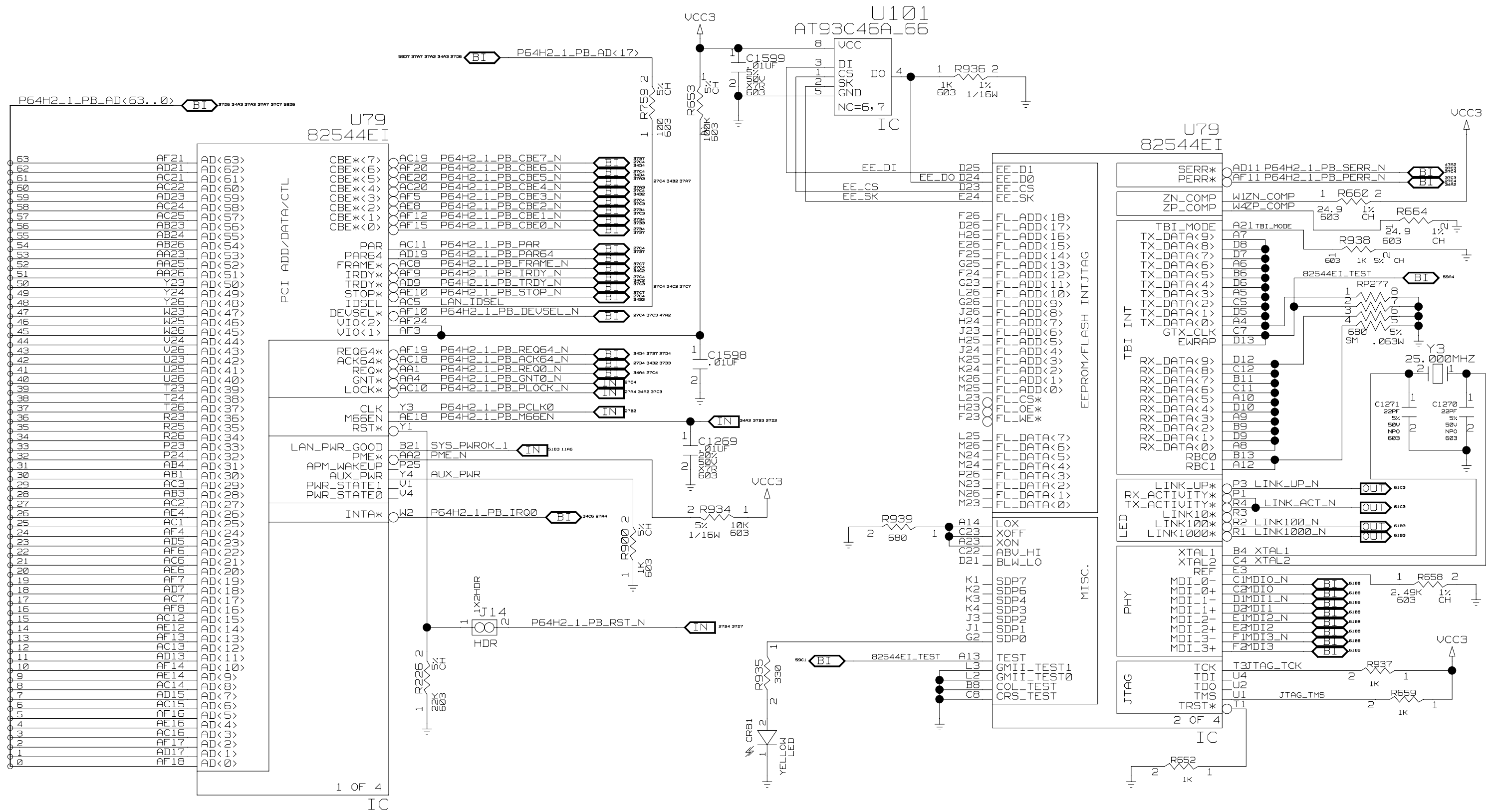


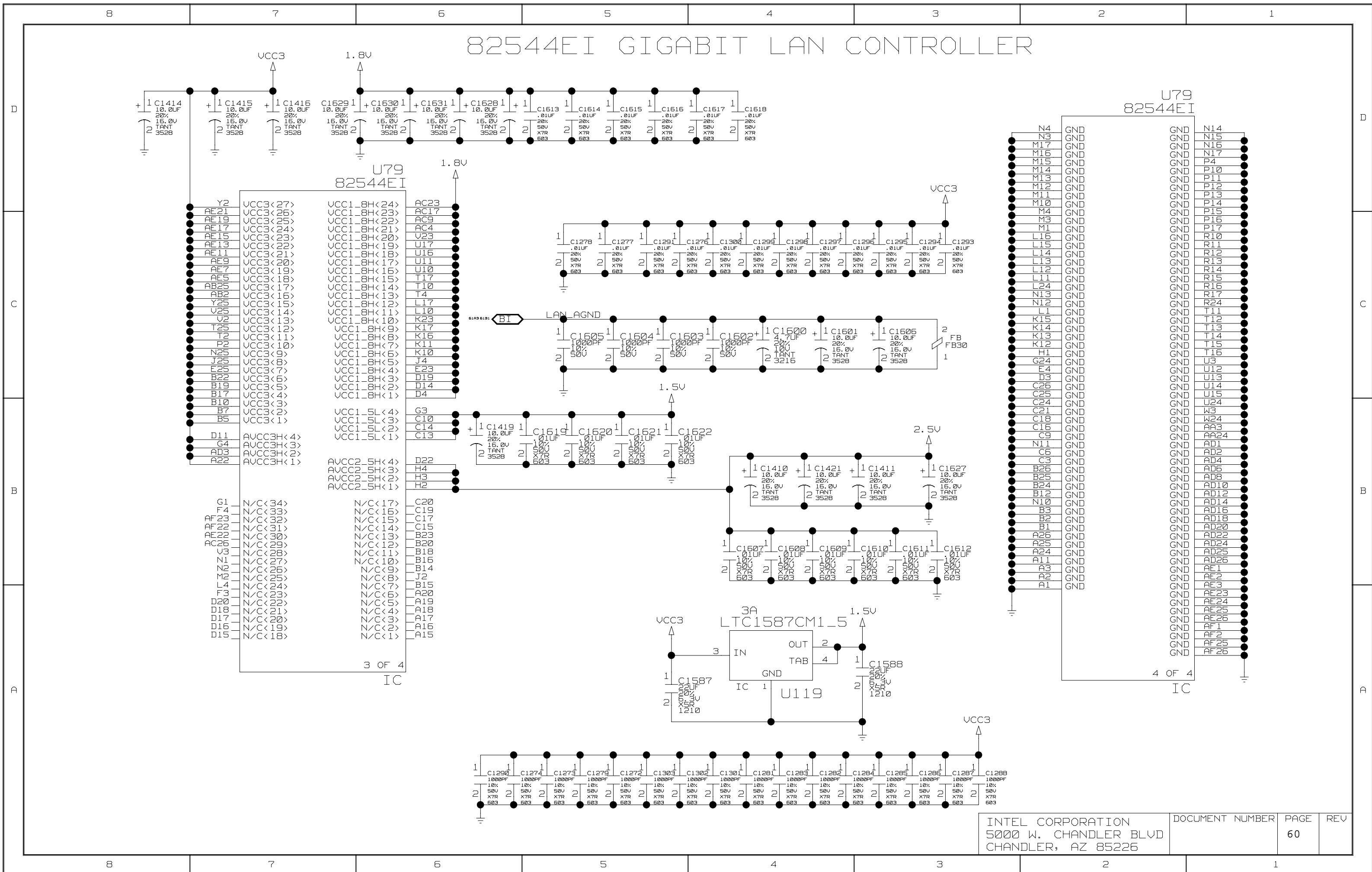
V1.2 REGULATION

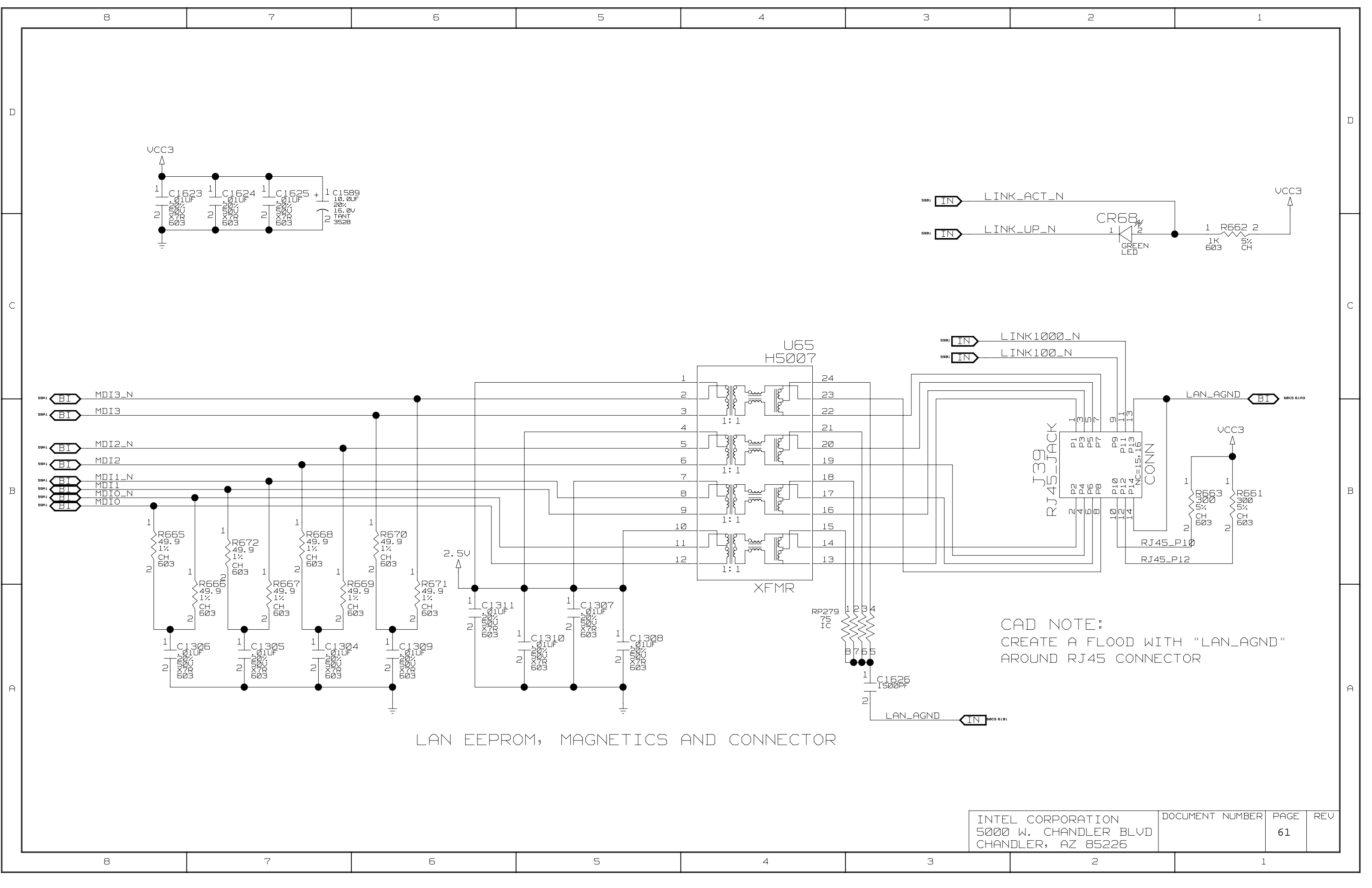
NOTE: ROUTE AS DIFFERENTIAL PAIR



82544EI GIGABIT LAN CONTROLLER





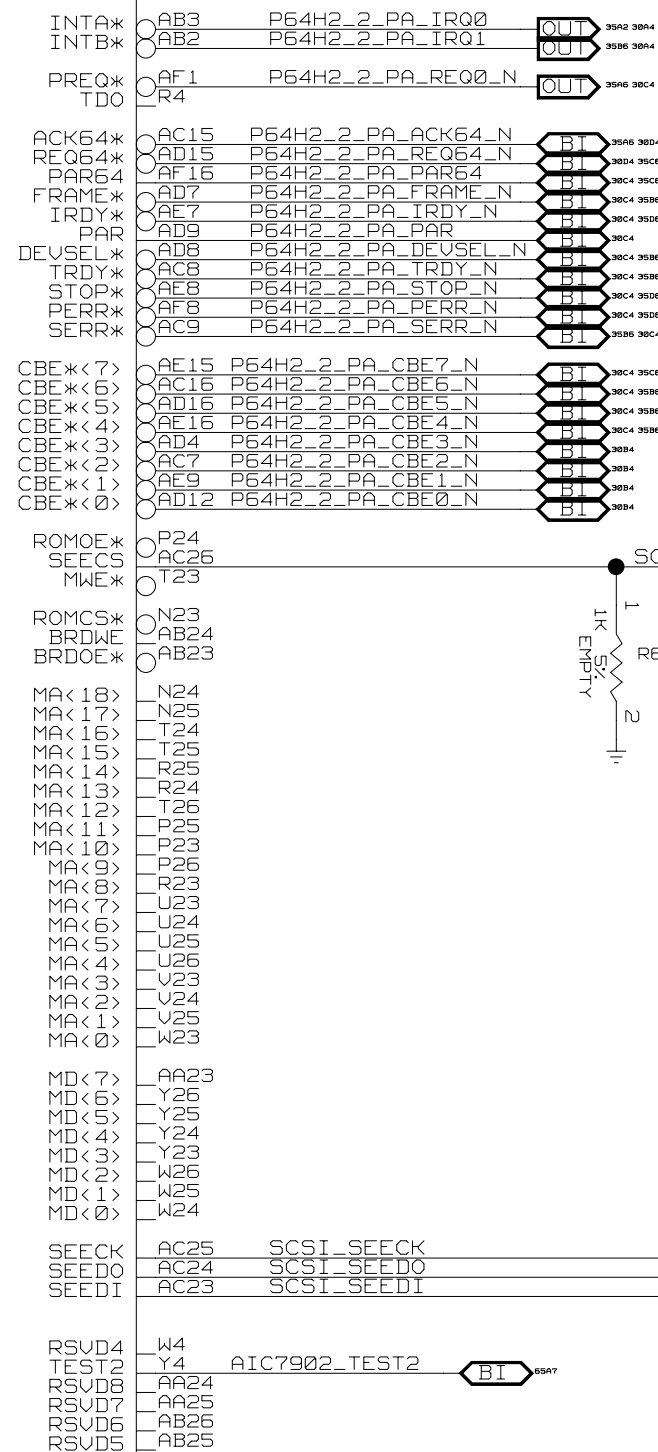


LAN EEPROM, MAGNETICS AND CONNECTOR

CAD NOTE:
CREATE A FLOOD WITH "LAN_AGND"
AROUND RJ45 CONNECTOR

SCSI CONTROLLER

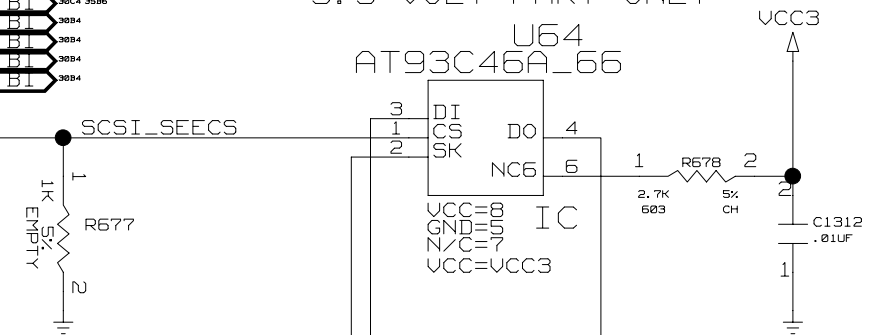
U78
AIC_7902A



SEE ADAPTEC* AIC-7902
DESIGN-IN HANDBOOK FOR
INFORMATION REGARDING
SEEPROM IMPLIMENTATION

3.3 VOLT PART ONLY

U64
AT93C46A_66



SAME AS AIC7902

1 OF 6

IC

*Other names and brands may be claimed as the property of others.

INTEL CORPORATION
5000 W. CHANDLER BLVD
CHANDLER, AZ 85226

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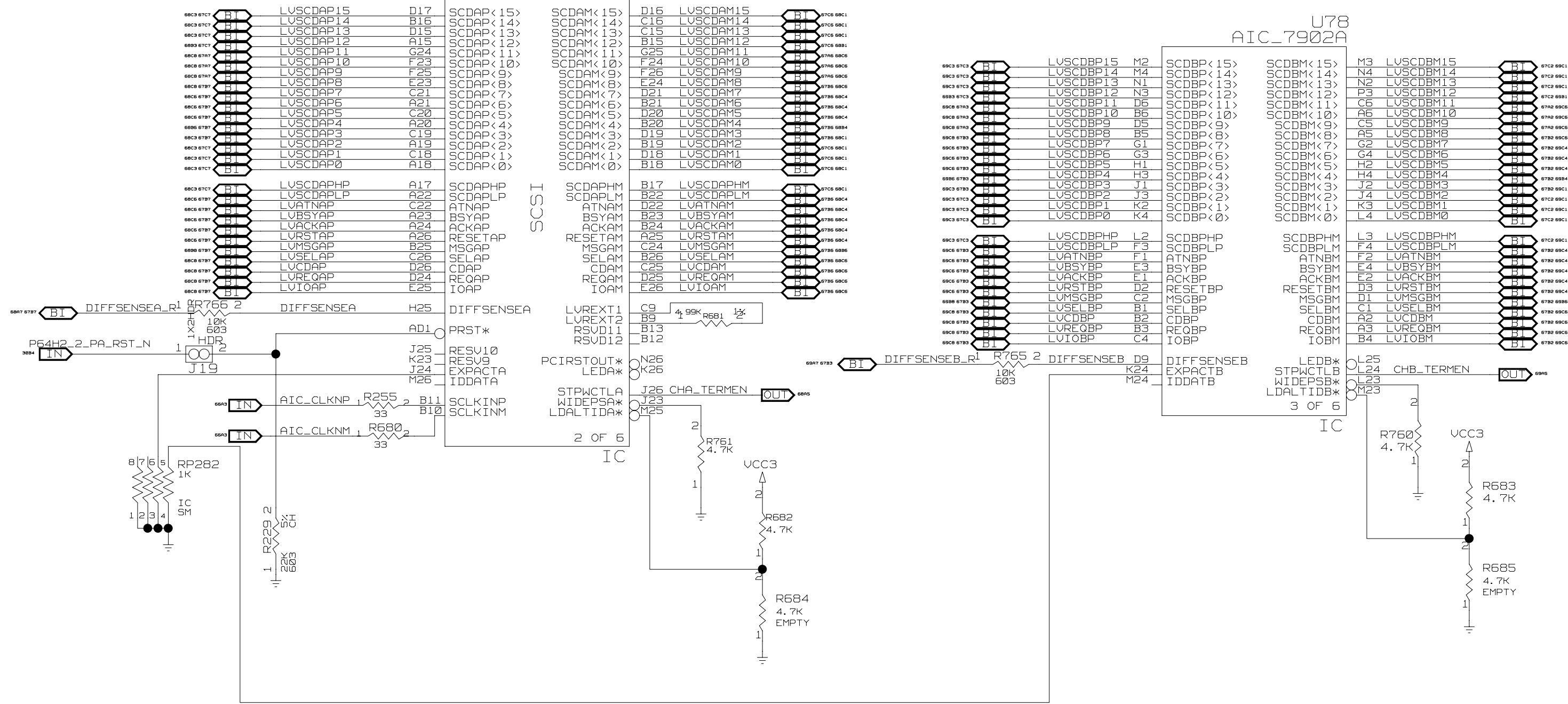
SCSI CONTROLLER

U78
AIC_7902A

U78
AIC_7902A

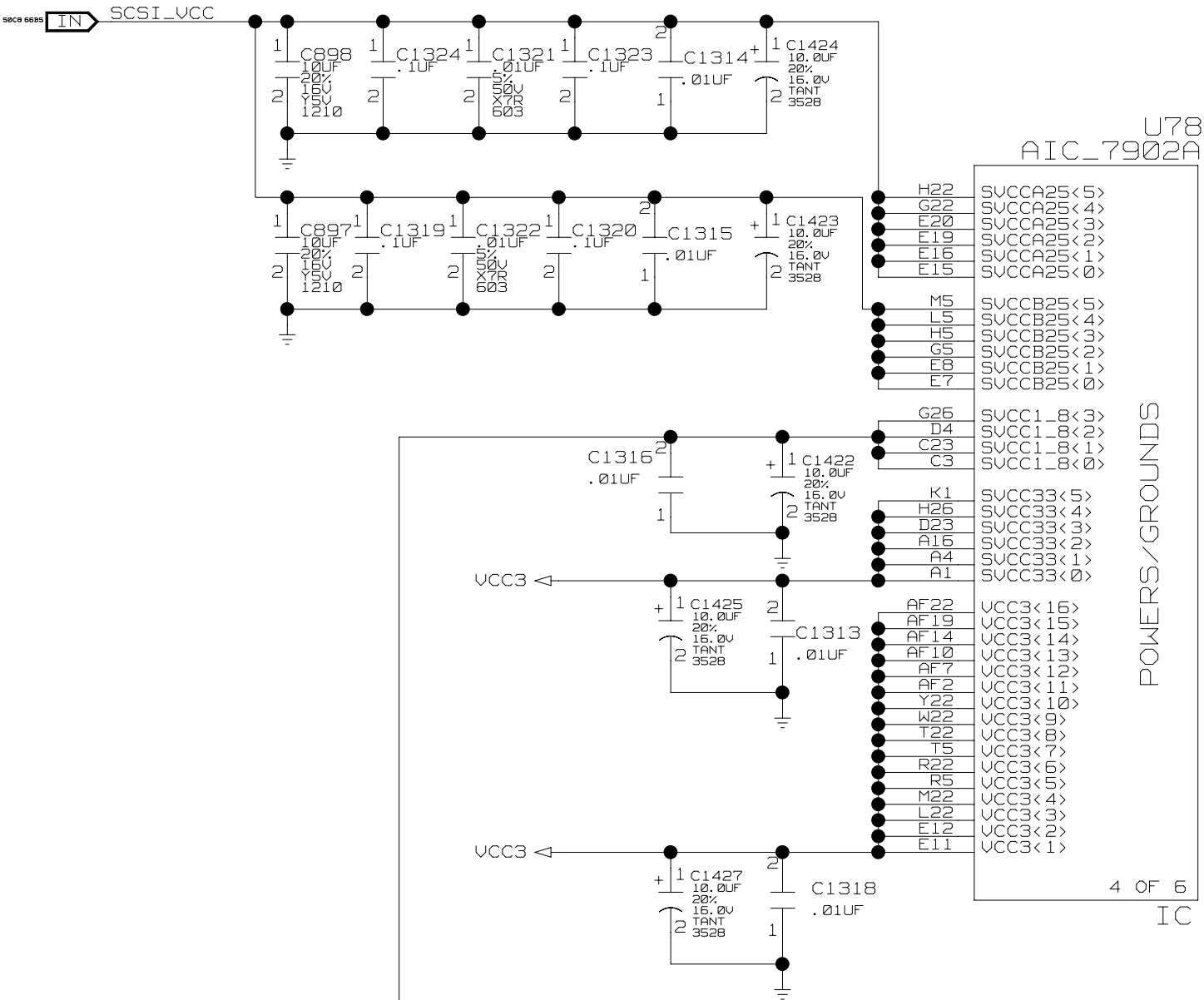
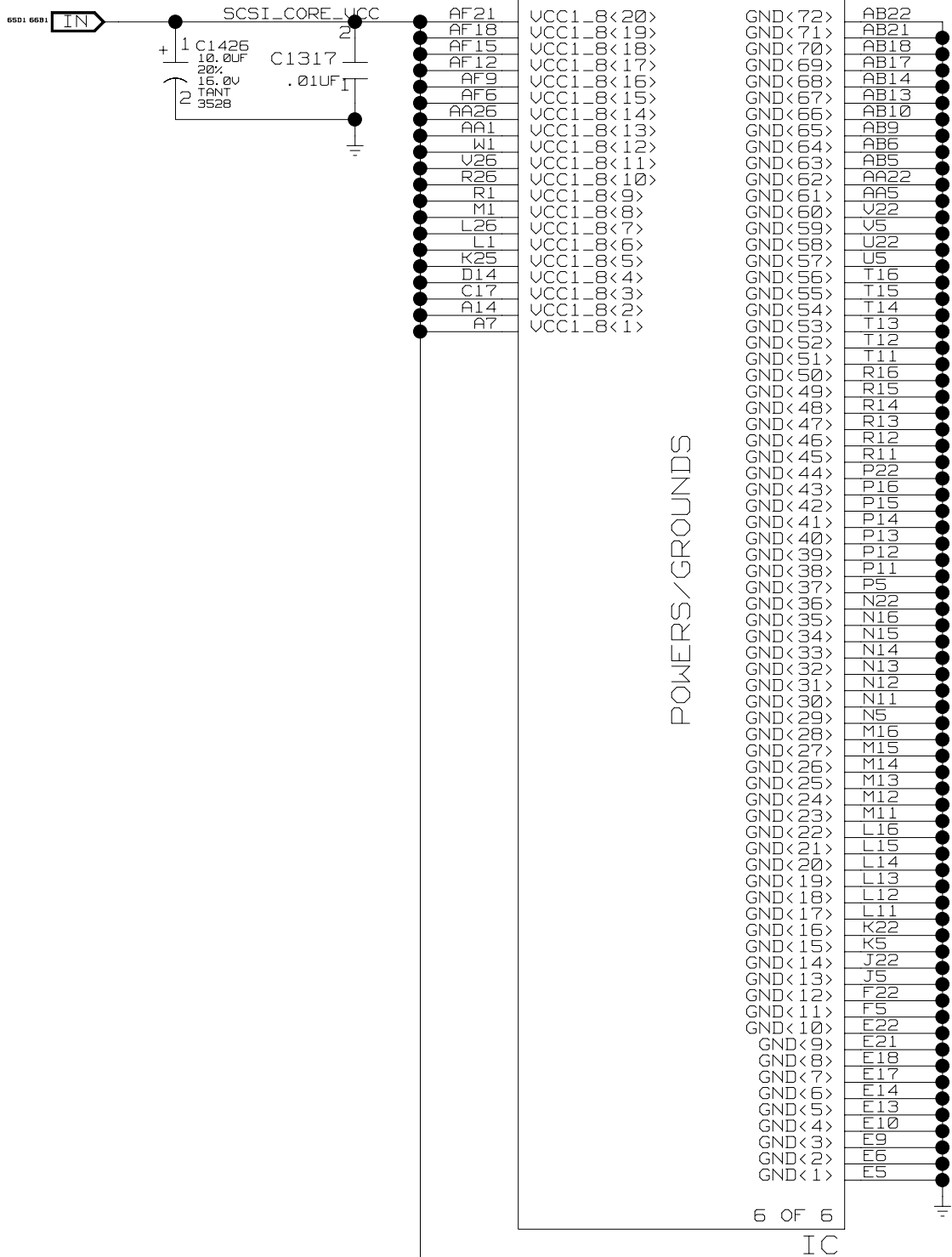
SCSI

IC

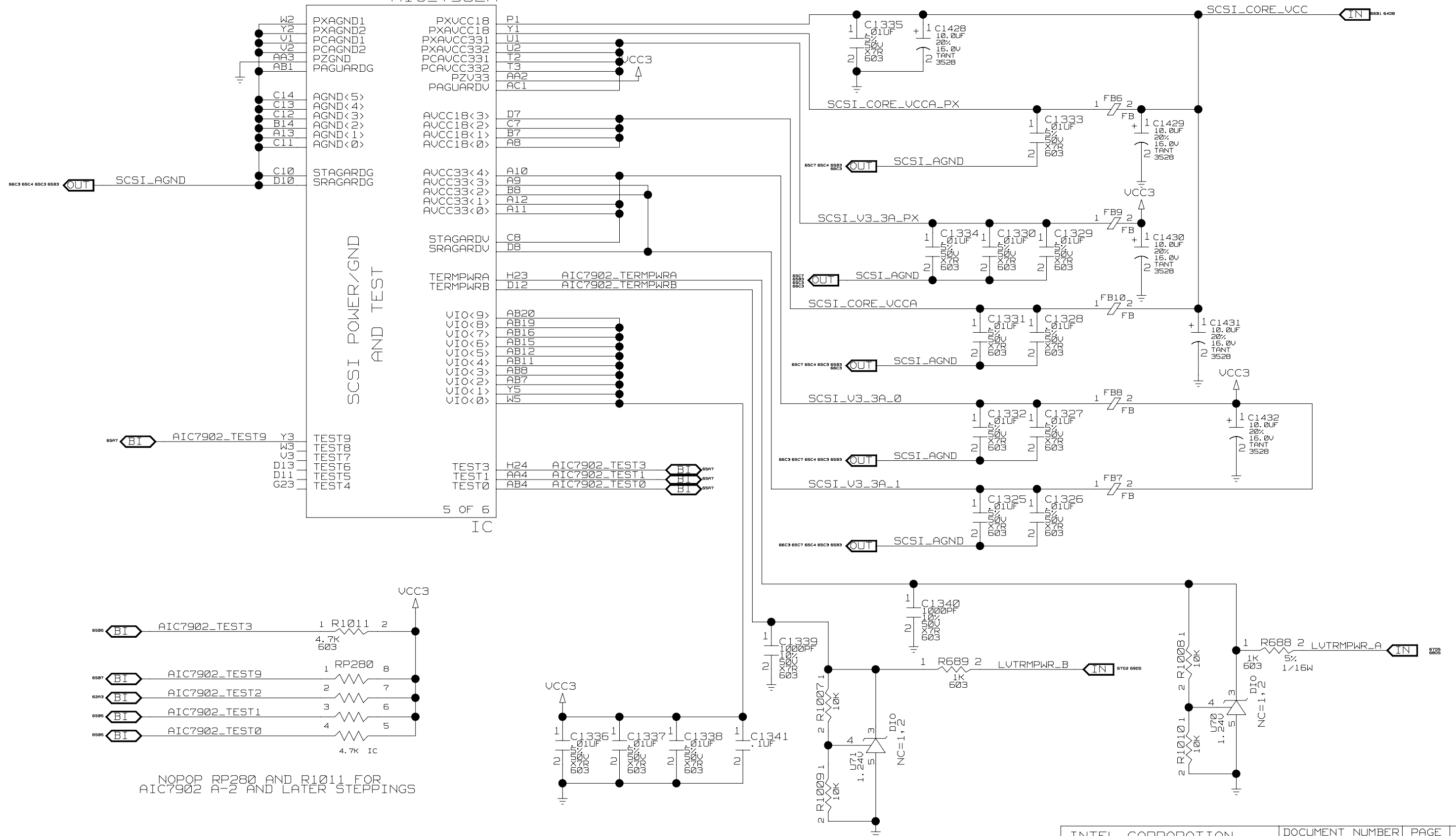


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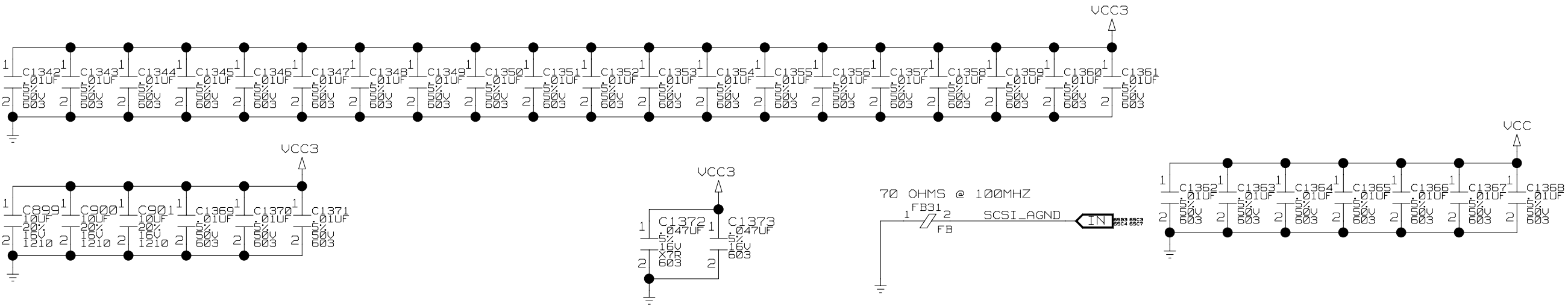
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U78
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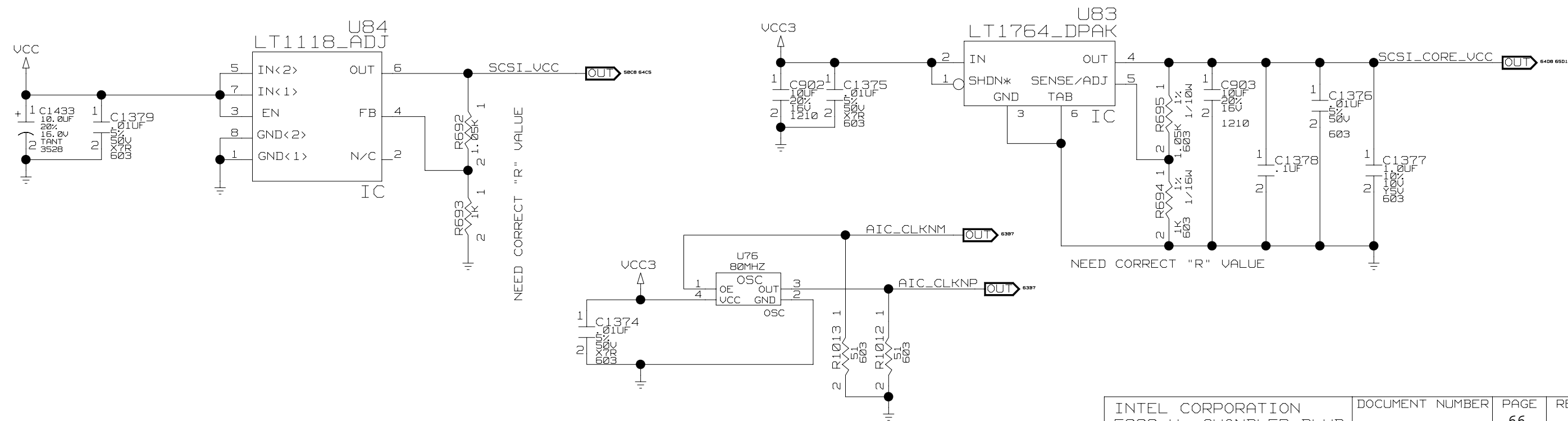


AIC - 7902 SCSI DECOUPLING RECOMMENDATION FOR POWER SUPPLIES

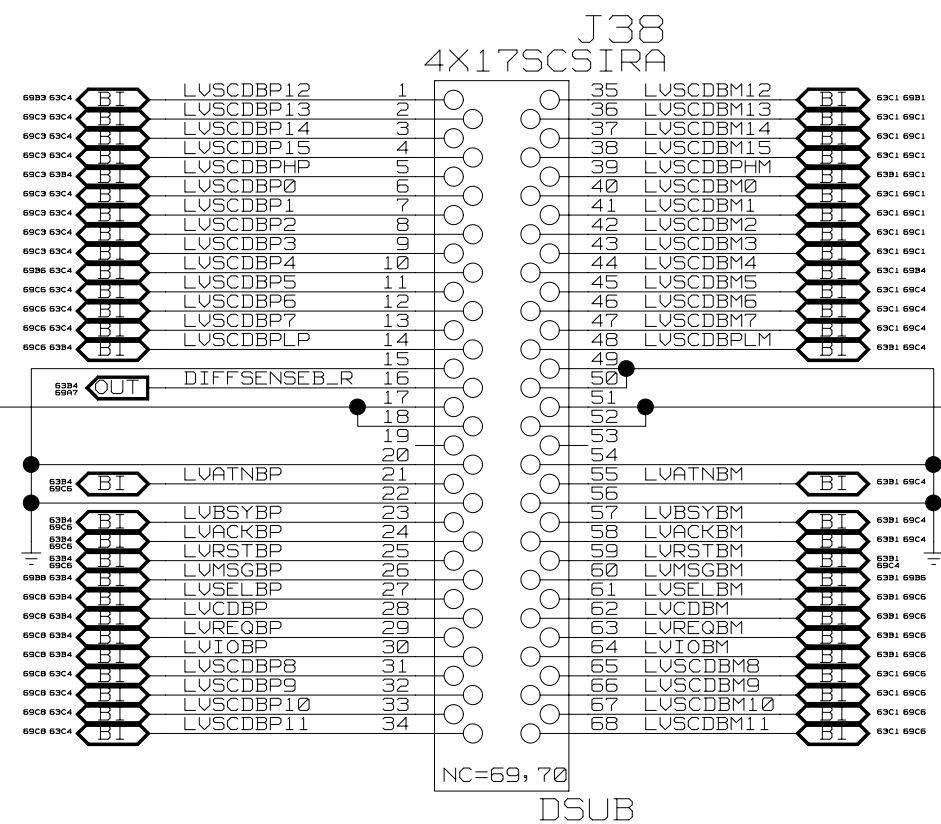
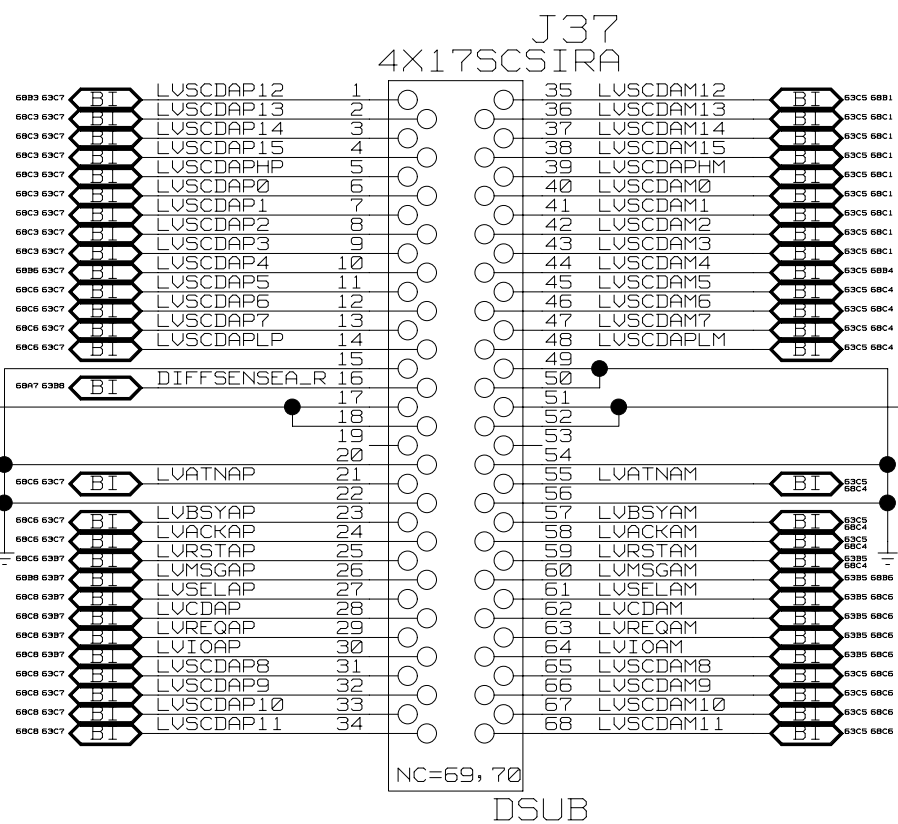
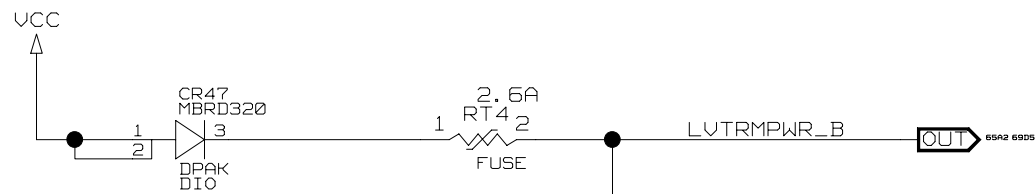
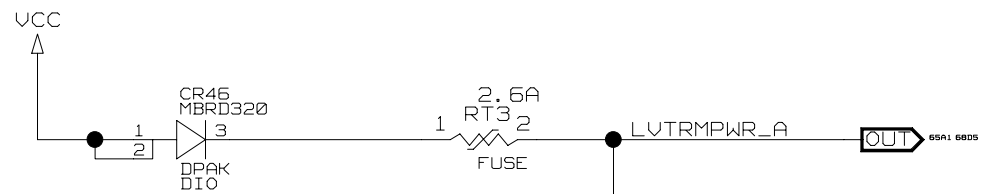


ISOLATE DIGITAL & ANALOG GROUND

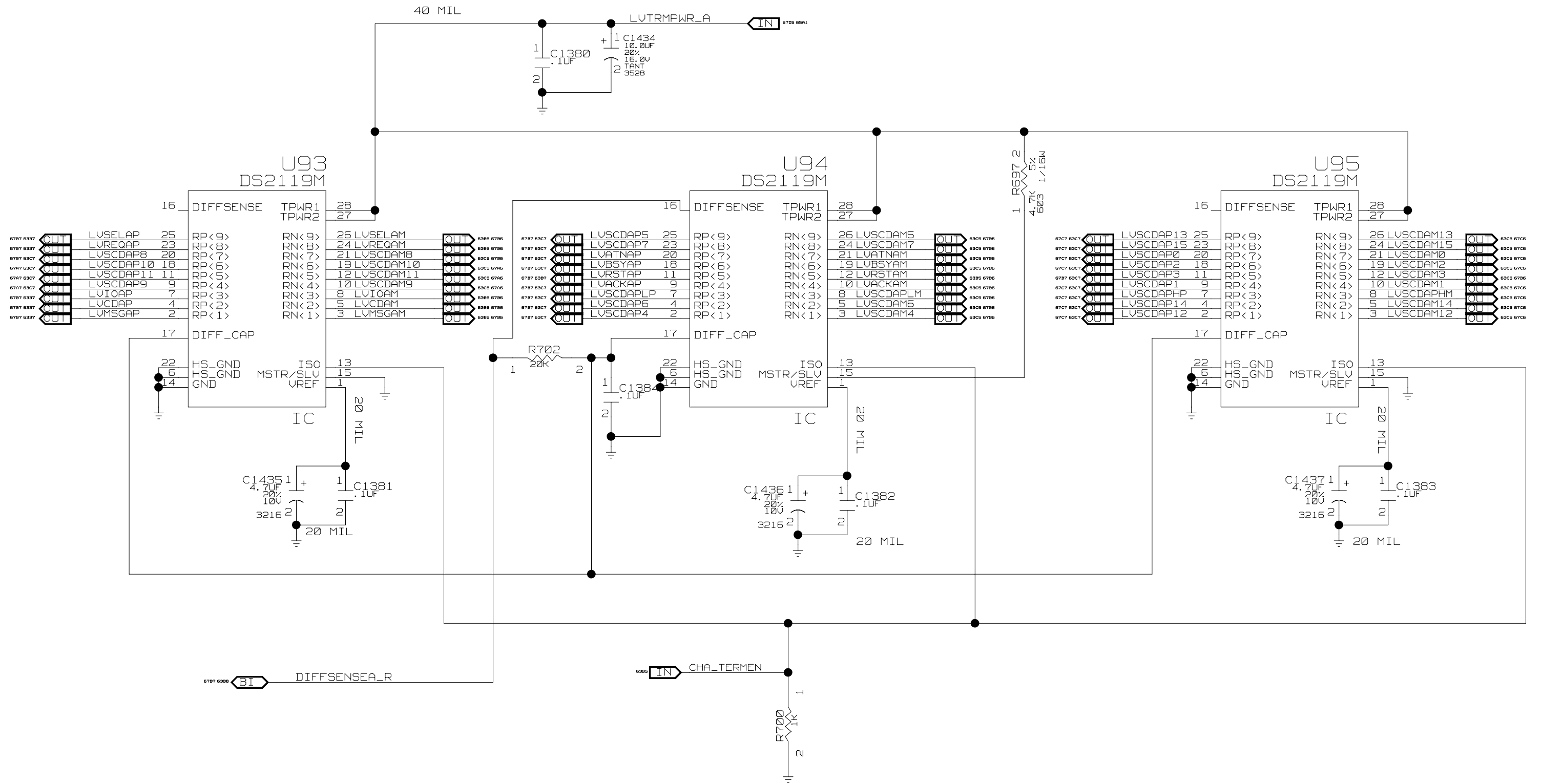
VOLTAGE REGULATORS AND SCSI CLOCK



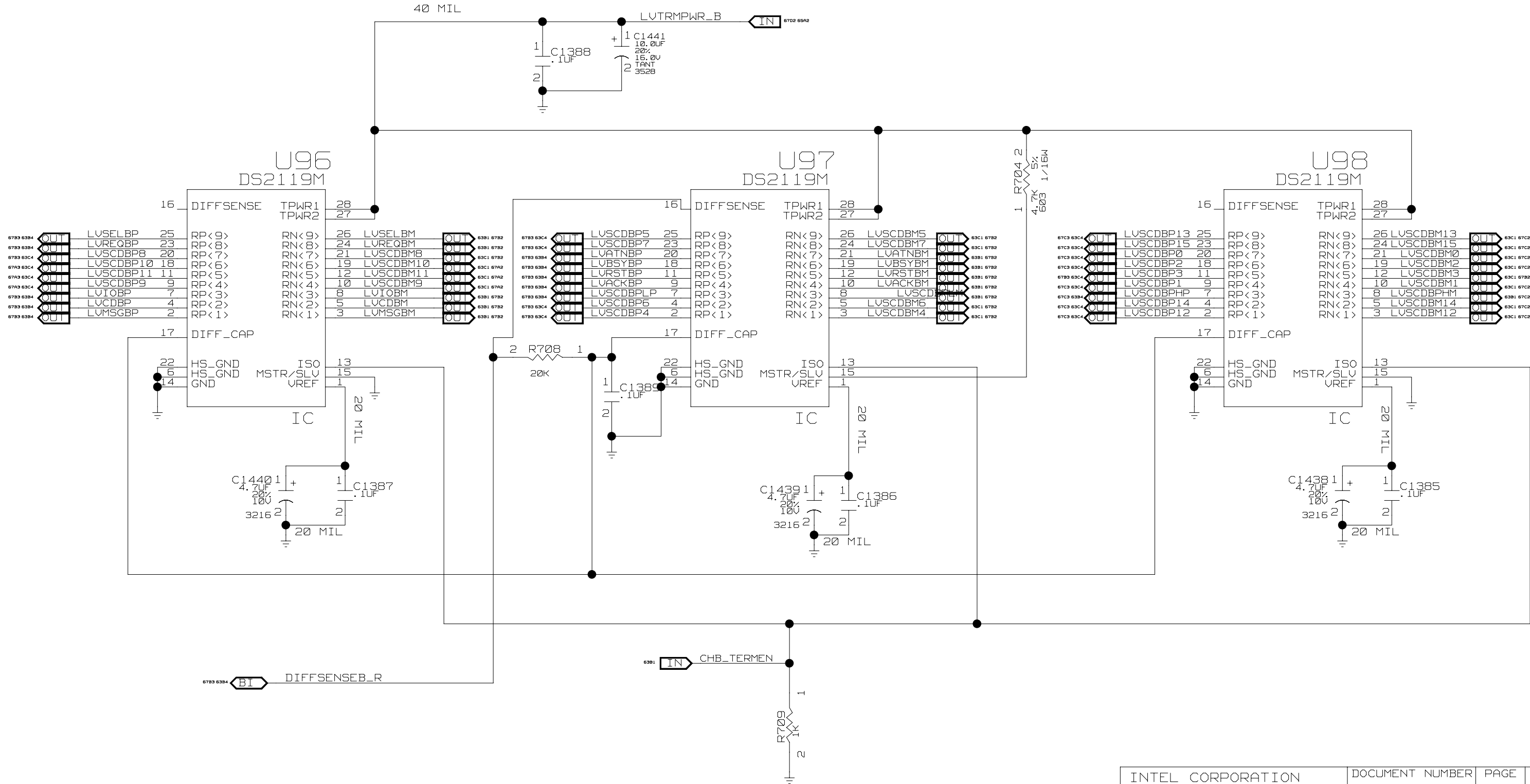
SCSI CONNECTORS A AND B

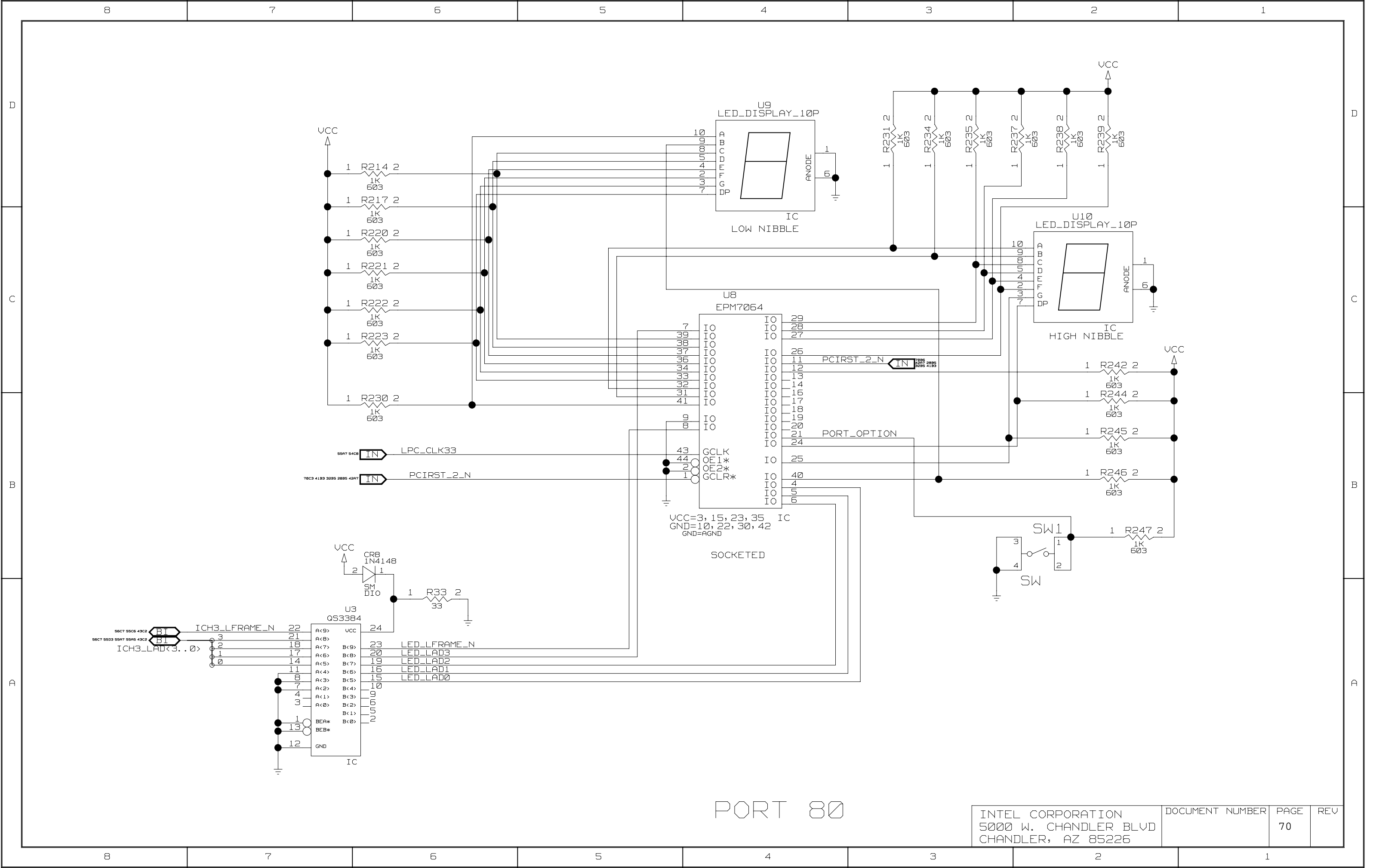


LVD/SE TERMINATION FOR SCSI CHANNEL A

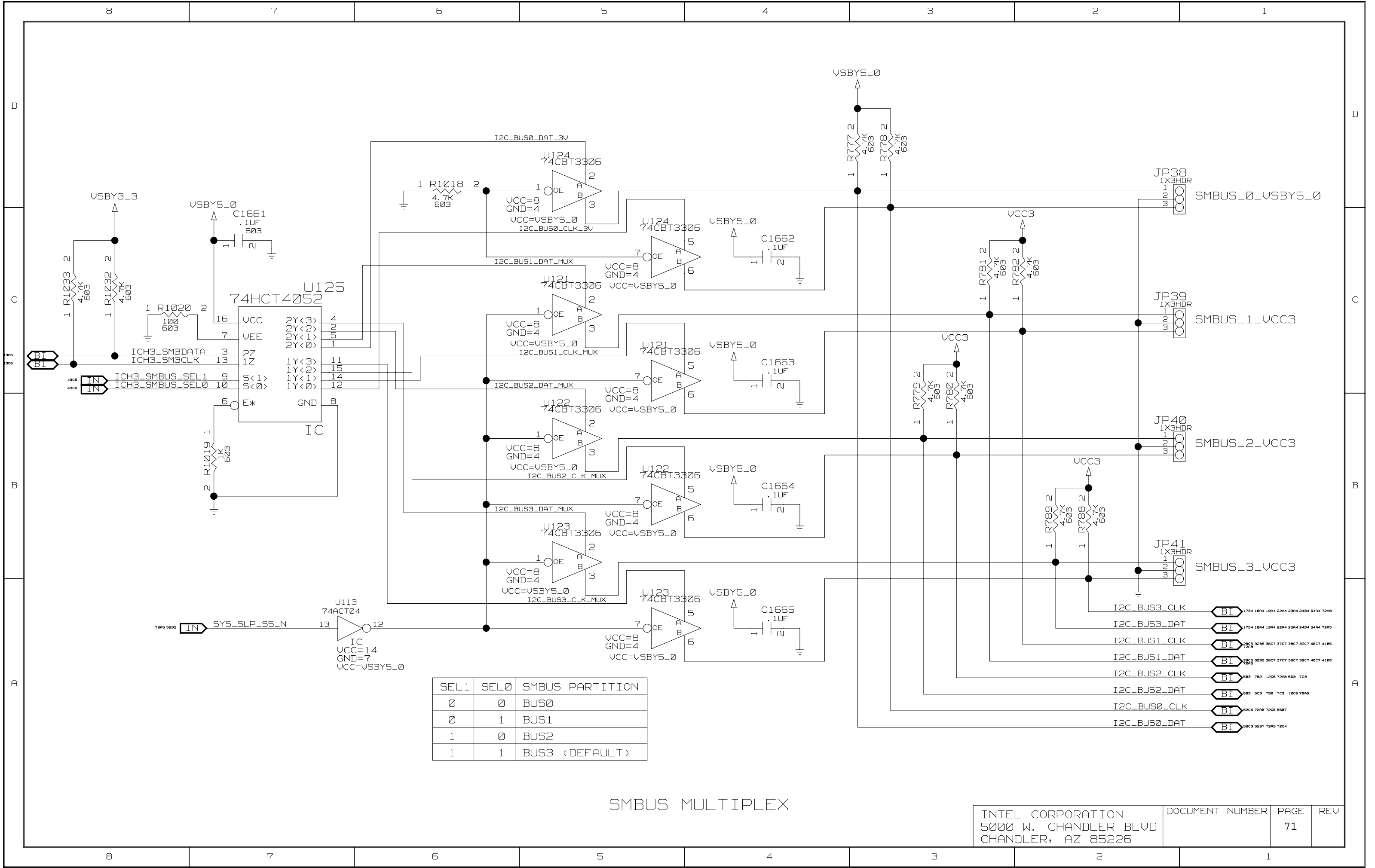


LVD/SE TERMINATION FOR SCSI CHANNEL B

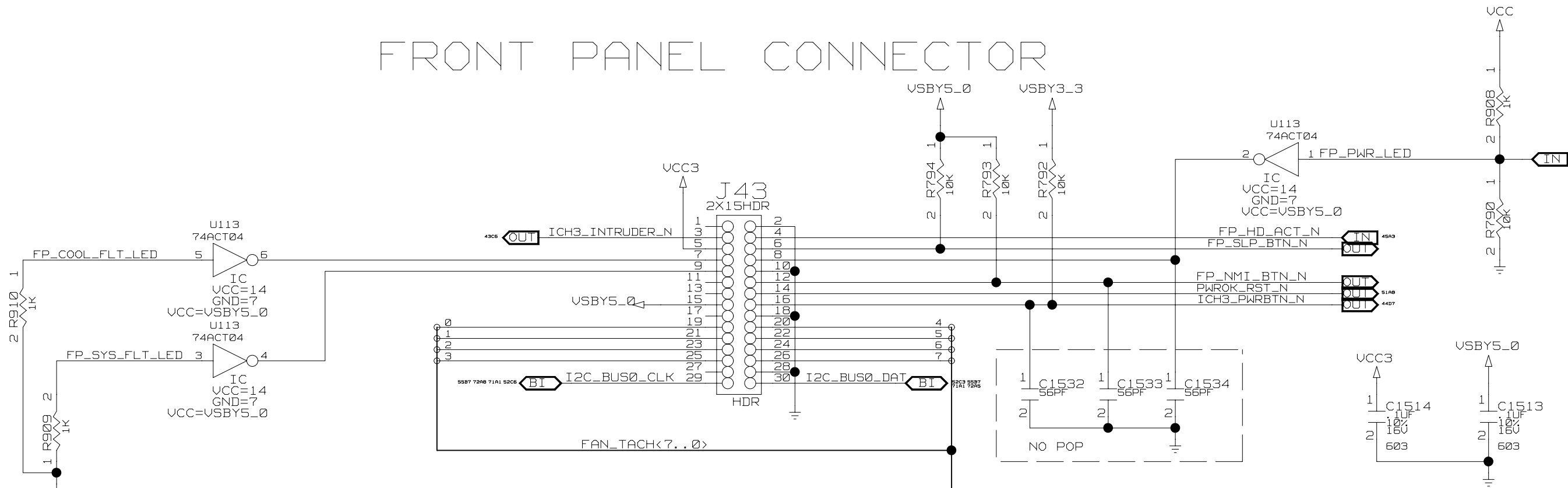




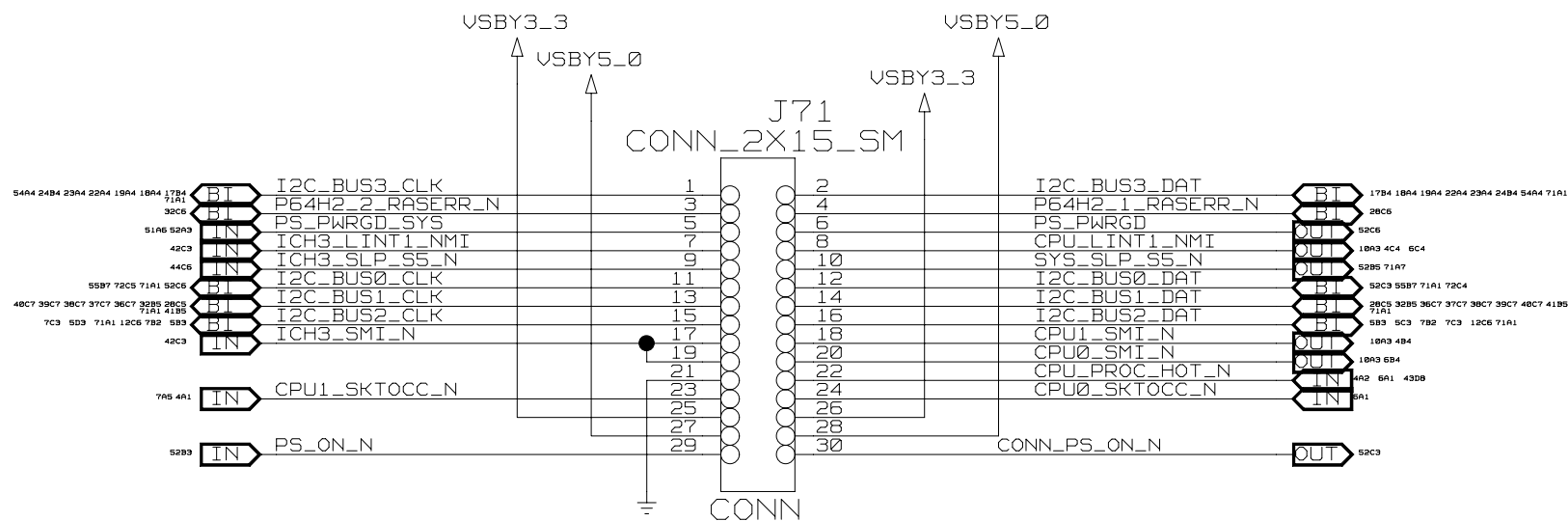
PORT 80



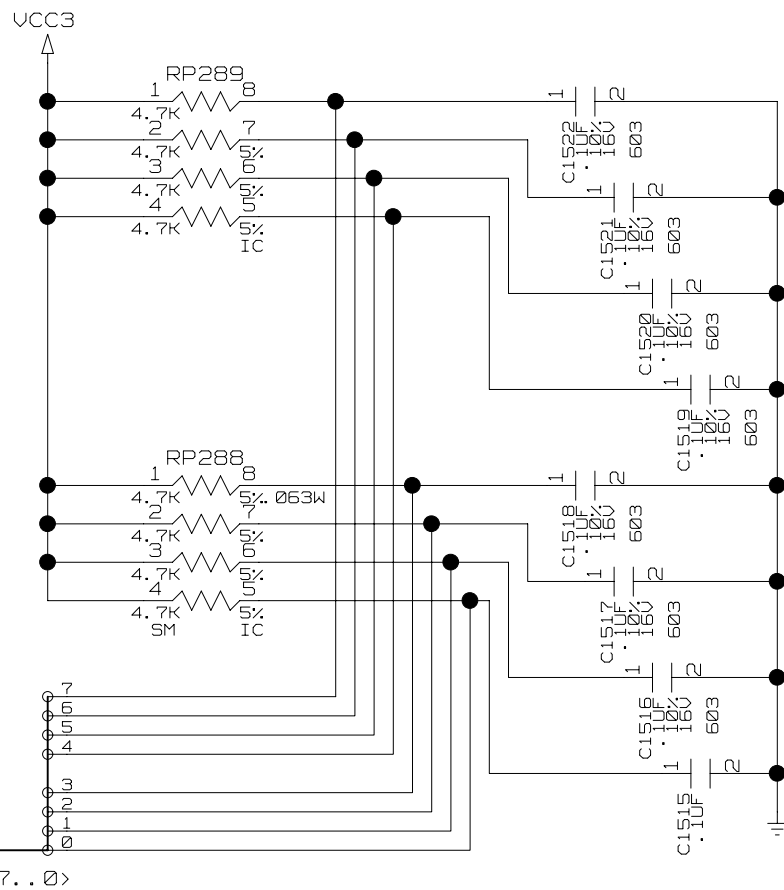
FRONT PANEL CONNECTOR



BMC CONNECTOR FOR VALIDATION



INSTALL JUMPERS TO SHORT PIN PAIRS:
5-6, 7-8, 9-10, 17-18, 19-20, 29-30



D

C

B

A

D

C

B

A

8

7

6

5

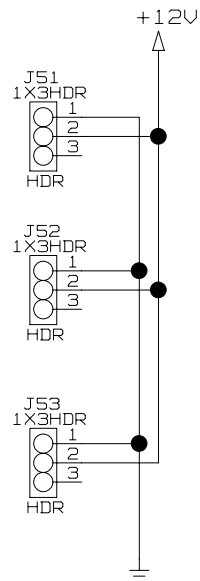
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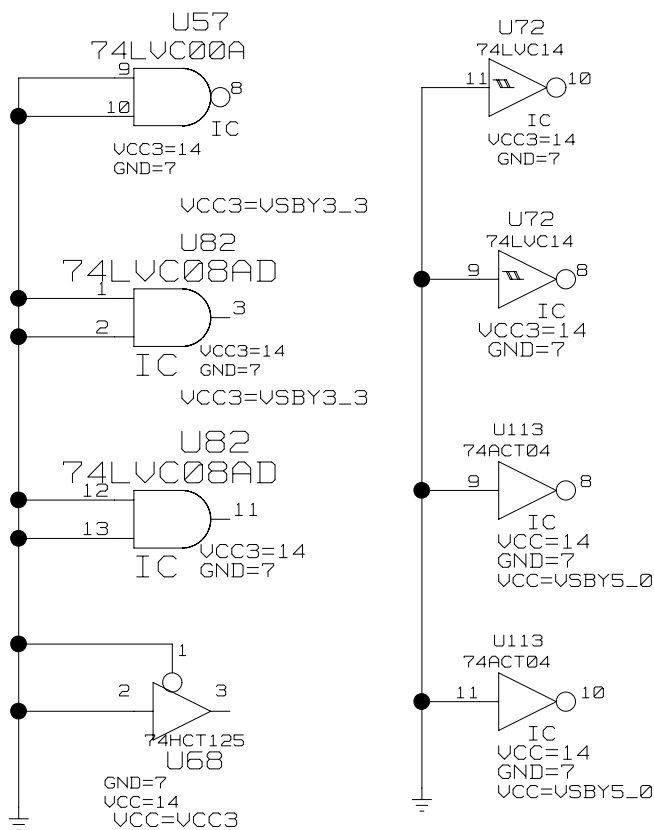
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1

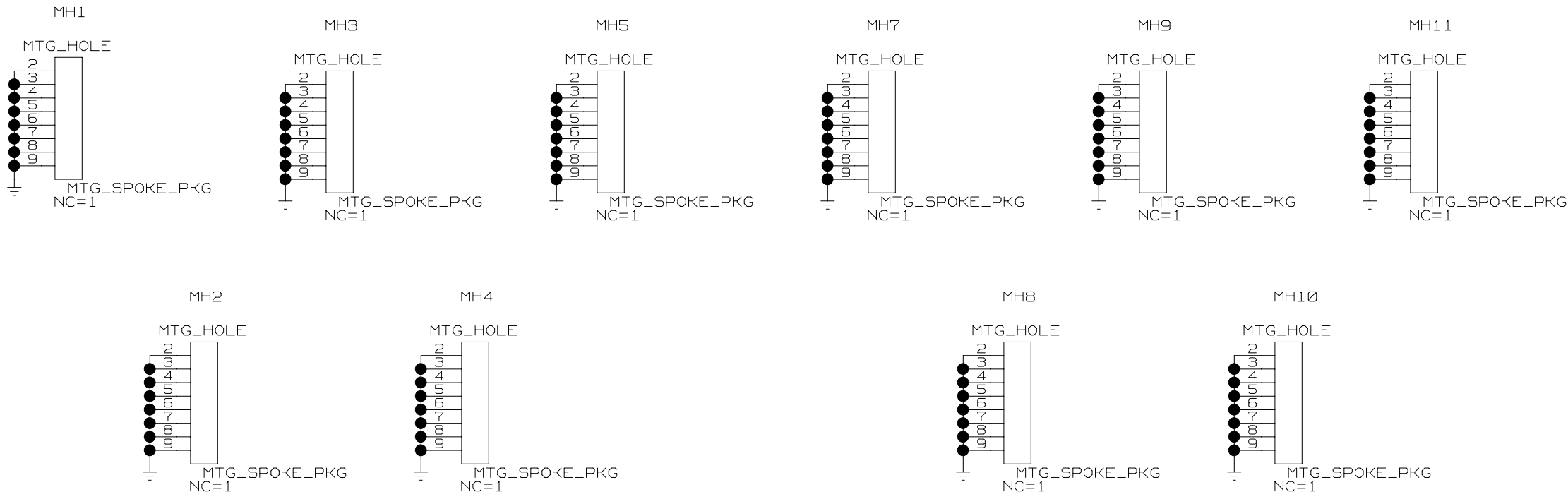
FAN HEADERS



SPARE GATES



MOUNTING HOLES



8

7

6

5

4

3

2

1